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MANUAL of Operating & Maintenance Procedures for

Series 2000

Digital Multimeter

Model 2500

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DATA PRECISION
... years ahead

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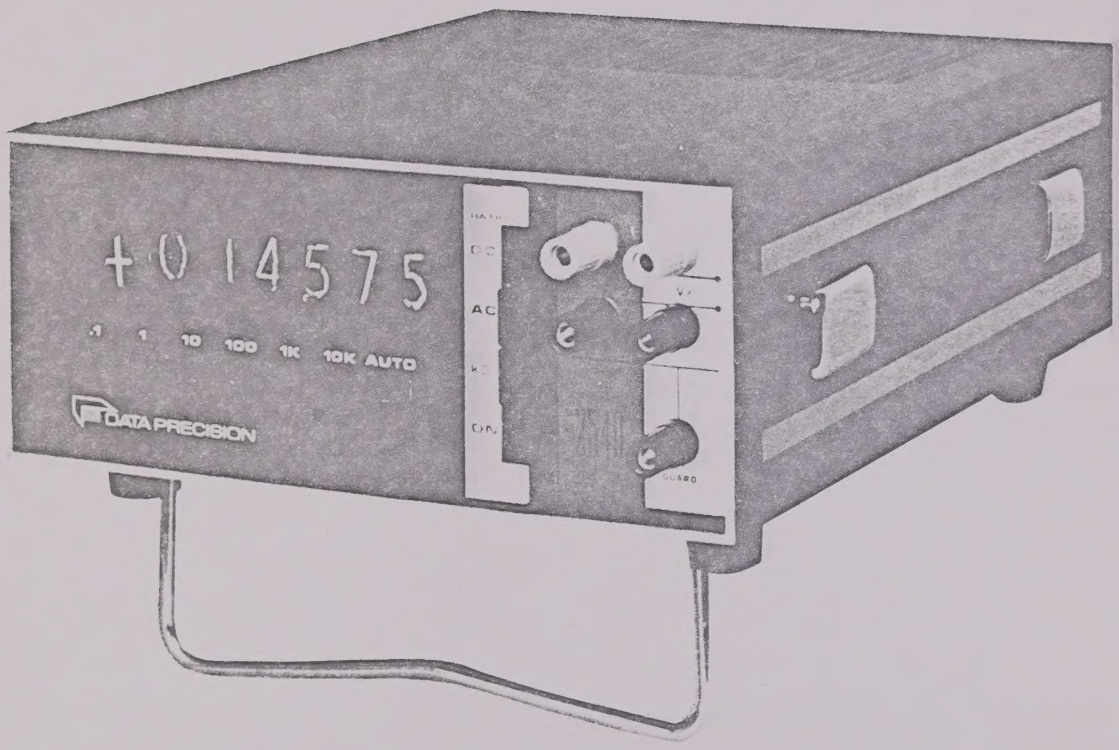

Frontispiece. SERIES 2000 DMM Model 2500

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Section 1
INTRODUCTION

The Series 2000 Digital Multimeter is the first implementation of a new concept in digital instrumentation. It features:

TRI-PHASIC™ A/D Conversion,
ISO-Polar™ Reference Generation, and
Ratiohmic™ Resistance Measurements.

The new design concepts have resulted in a marked increase in technical performance at radically reduced cost.

Every Series 2000 Digital Multimeter includes full capabilities for:

- Auto-Ranging for all measurements, which automatically selects the range scale of highest resolution for the input signal (Manual ranging is also included);
- BCD Outputs, which remain latched between conversions and which are available for remote data output;
- Overload Indicator, which enables the system user to reject invalid measurement indications;
- Remote Control, which enables the system user to trigger measurement cycles according to his needs and to change the range on external command.

The measurement functions incorporated in each Model are listed below. The complete specifications for the 5-1/2 and 4-1/2 digit models are reproduced in the tabular data that follows.

5-1/2 Digit 2500 Series

Model	DC Volts	AC Volts	Ohms	DC Ratio
2540	X	X	X	X
2535	X	X		X
2530	X		X	X
2520	X			X

4-1/2 Digit Series

Model	DC Volts	AC Volts	Ohms	DC Ratio
2440	X	X	X	X
2435	X	X		X
2430	X		X	X
2420	X			X

Scope of Instruction Manual for MODEL 2500

This Instruction Manual for Model 2500 DMM contains the general description, principles of operation, operating and maintenance procedures, reference schematics, and parts lists.

NOTICE

The information contained herein is derived in part from proprietary and patent data of the Data Precision Company and its presentation in this Instruction Manual is solely for the assistance of equipment operating and maintenance personnel. Publication of this information does not convey any rights to reproduce or to use the information for any purpose other than in connection with the installation, operation, and maintenance of the equipments described herein.

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SPECIFICATIONS MODEL 2500 DMM

AC Volts

Nominal Range	Overrange	Resolution
1.00000	1.19999	10 μV
10.0000	11.9999	100 μV
100.000	119.999	1 mV
1000.00*	1000.00*	10 mV

*See maximum voltage limitation, below

Input Impedance (all ranges): 1 megohm in parallel with 100pF or less.

Sensing & Calibration: True-Average sensing, calibrated in RMS of sinewave.

Accuracy (6 months, 23°C ±5°C): See curve and specific ratings below.

Temperature Coefficient (0°C to 50°C, all ranges):
30Hz – 1kHz (±0.005% rdg. ±0.002% f.s.)/°C
1kHz – 10kHz (±(0.005 × freq. in kHz)% rdg. ±0.002% f.s.)/°C
10kHz – 100kHz (±0.05% rdg. ±0.002% f.s.)/°C

Maximum Input Voltage (sinewave RMS):
30Hz to 10kHz: 500V
above 10kHz: decreases linearly to 100V at 100kHz

Settling Time (to settle within ±0.05% of final reading for a full-scale step input): 2.5 seconds.

DC Volts

Nominal Range	Overrange	Resolution	Input Impedance	Maximum Voltage
±1.00000	±1.19999	10μV	>1,000 megohms	1000V
±10.0000	±11.9999	100μV	>1,000 megohms	1000V
±100.000	±119.999	1mV	10 megohms	1000V
±1000.00	±1000.00	10mV	10 megohms	1000V

Accuracy (all ranges, including overrange):
24 hours, 23°C ±1°C ±0.004% rdg ±0.001% f.s. ±1 l.s.d.
6 months, 23°C ±5°C ±0.007% rdg ±0.001% f.s. ±1 l.s.d.
Add ±0.00001% rdg/Volt.

Temperature Coefficient (0°C to 50°C, all ranges):
(±0.001% rdg ±0.0002% f.s.)/°C

Common-Mode Rejection Ratios (minimum):
at DC, 160dB with 1000Ω source-impedance unbalance
at 60Hz, 120 dB with 1000Ω source-impedance unbalance

Common-Mode Voltage: 250V DC (or AC peak) maximum.

Normal-Mode Rejection Ratio: 60dB at 10Hz and all integral multiples thereof.

OPTION A1:

Nominal Range	Overrange	Resolution	Input Impedance	Maximum Voltage
±100000	±119999	1μV	>1,000 megohms	1000V

Accuracy:
24 hours, 23°C ±1°C ±0.005% rdg ±0.004% f.s. ±1 l.s.d.
6 months, 23°C ±5°C ±0.008% rdg ±0.004% f.s. ±1 l.s.d.

Temperature Coefficient (0°C to 50°C):
(±0.001% rdg ±0.001% f.s.)/°C

Ohms

Nominal Range	Overrange	Resolution	Max Test Current
1.00000kΩ	1.19999kΩ	10 milliohms	1 mA
10.0000kΩ	11.9999kΩ	100 milliohms	100 μA
100.000kΩ	119.999kΩ	1 Ohm	10 μA
1.00000 meg Ω	1.19999 meg Ω	10 Ohms	1μA
10.0000 meg Ω	11.9999 meg Ω	100 Ohms	0.1 μA

Configuration: True four-wire.

Maximum Open Circuit Voltage: 6.2 Volts.

Accuracy (6 months, 23°C ±5°C):
1kΩ/10kΩ/100kΩ ranges ±0.007% rdg ±0.001% f.s. ±1 l.s.d.
1 meg Ω range ±0.02% rdg ±0.002% f.s. ±1 l.s.d.
10 meg Ω range ±0.2% rdg ±0.01% f.s. ±1 l.s.d.

Temperature Coefficient (0°C to 50°C):
1kΩ/10kΩ/100kΩ ranges (±0.001% rdg ±0.0004% f.s.)/°C
1 megΩ range (±0.005% rdg ±0.0004% f.s.)/°C
10 megΩ range (±0.02% rdg ±0.005% f.s./°C

Settling Time (to settle to within ±0.01% fo final reading):
1kΩ/10kΩ/100kΩ ranges 0.1 sec.
1 megΩ range 0.4 sec.
10 megΩ range 3.1 sec.

Settling Time in seconds for any resistance = 0.1 + 0.3 x Resistance in Megohms.

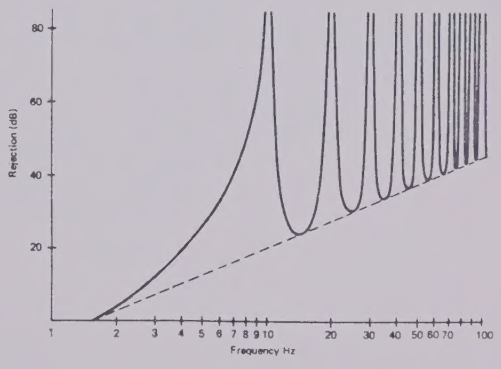

Figure 1-1. Common Mode Rejection

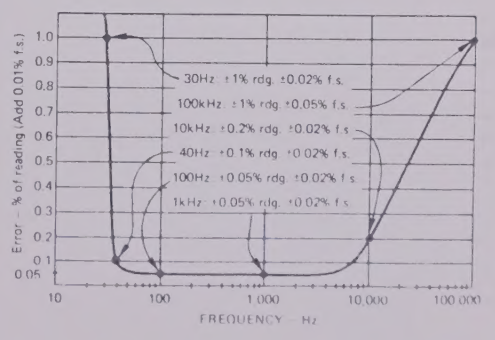

Figure 1-2 Series 2000 DMM AC-Volt Accuracy

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SPECIFICATIONS MODEL 2500 DMM (Continued)

DC Ratio

Selected Range	Nominal Range	Overrange	Actual Display*
1	±.100000:1	±.119999:1	±1.19999
10	±1.00000:1	±1.19999:1	±11.9999
100	±10.0000:1	±11.9999:1	±119.999
1000	±100.000:1	±119.999:1	±1199.99

*Displayed Ratio is 10 times true ratio

Accuracy:

24 hours, 23° ±1°C:

$$[\pm 0.004\%\ \text{rdg} \pm 0.001\%\ \text{f.s.} \pm 1\ \text{l.s.d.}] \times \frac{10}{\text{Actual Ref. Voltage}}$$

6 months, 23°C ±5°C:

$$[\pm 0.008\%\ \text{rdg} \pm 0.001\%\ \text{f.s.} \pm 1\ \text{l.s.d.}] \times \frac{10}{\text{Actual Ref. Voltage}}$$

Temperature Coefficient (0°C to 50°C, all ranges):

$$[\pm 0.001\%\ \text{rdg} \pm 0.0002\%\ \text{f.s.}] \times \frac{10}{\text{Actual Ref Voltage}} /°C$$

Voltage Coefficient of Ratio: ±0.00001% rdg/Volt

Voltage Range:

Input Signal: 0 to ±1000V
Reference Signal: +1V to +11V

Reference Input Impedance: 100kΩ

Common-Mode Rejection Ratio: Same as DC Volts

Normal Mode Rejection Ratio: Same as DC Volts

Interface & Application Specifications

Signal Interfaces.

Data Outputs (DTL/TTL compatible) BCD 1-2-4-8 coded positive true
Logic ONE: > +2.4V
Logic ZERO: < +0.4V sink for 4mA
Polarity output, ONE = Positive polarity

State Outputs (DTL/TTL compatible)
Range in use = ZERO: < +0.4 sink for 4mA
Inactive ranges = ONE: > +2.4V
End of Conversion is transition from ZERO to ONE.

Control Inputs.

Range Each range is selected by the grounding of the appropriate line, through switch contacts or grounded transistor.

External Trigger
Positive pulse 2.4 volts with a pulse width of >1μsec, and <100 msec will initiate a read command. The command will cause the instrument to perform one measurement. The reading will remain in the memory until a new external trigger pulse is initiated.

Trigger Enable Input (applying logic "0" inhibits conversion in all trigger modes)
Logic "1" > +2.4V
Logic "0" < +0.4V sink for 40mA

Input Power: 105V–125V AC (or 210–250V AC) at 47–430Hz, less than 12 Watts. Line-voltage range is selected by rear-panel switch.

Environment.

Temperature Ranges Operating, 0°C to +50°C
Storage, −25°C to +80°C

Humidity 95% RH max, 0°C to +40°C
80% RH max, +40°C to +50°C

Overall Dimensions: 3½" high, 8½" wide, and 12" deep, including panel controls and connectors.

Weight: 8 pounds net, 10 pounds packed for domestic shipment.

Stand: Adjustable, removable, tilt-up stand provided for best viewing in bench use.

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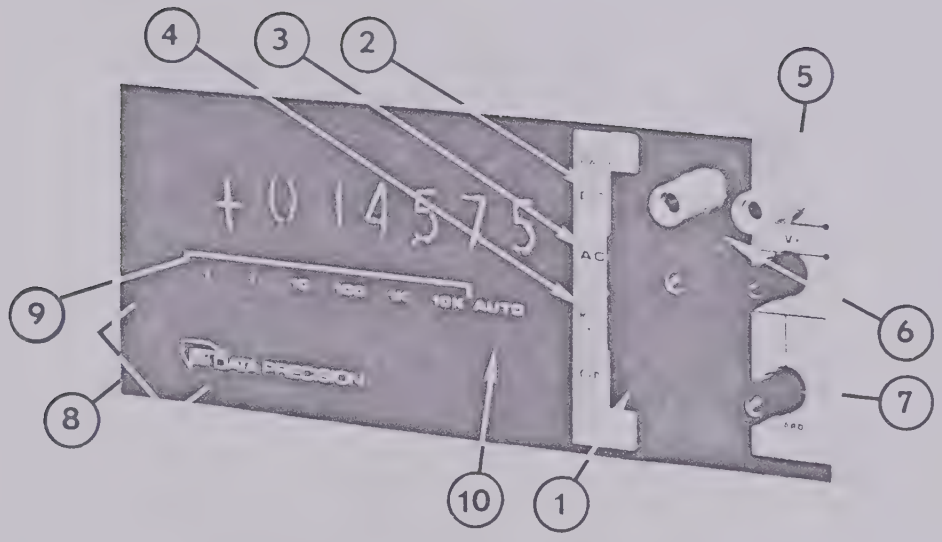

Figure 2-1. MODEL 2500 DMM Front Panel Controls and Indicators

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Table 2-1 (Continued)

FRONT PANEL CONTROLS AND INDICATORS

Fig. Ref.	Control/ Indicator	Description	Function
3.	AC	Push switch & light indicator	*Selects AC voltage measurement mode of DMM action. Is interlocked with other modes so that it is pushed out upon selection of another mode.
4.	kΩ	Push switch & light indicator	*Selects resistance measurement mode of DMM operation. Is interlocked with other modes so that it is pushed out upon selection of another mode.
5.	Vx	Two 5-way binding posts	Connection for input voltage, AC or DC, or resistance.
6.	Rx	Two 5-way binding posts	Current source and sink terminals for resistance connection. Connection for voltage ratio reference input.
7.	GUARD	One 5-way binding post	External connection to guard shield.
8.	DISPLAY	NIXIE Tube indicators	Displays digital readout for a maximum of 120000. Decimal point is selected automatically and appears in the appropriate NIXIE tube to indicate value of a direct reading. Sign is displayed automatically when in DC measurement mode.
9.	RANGE DC 0.1 1 10 100 1000 10000	Push switch for manual range selection	Selects value of full scale range to be used by DMM in measuring input. Is interlocked so that only one may be in at a time. 0.1 for use with option A1/A2. 10000 for use with kΩ function only.
10.	AUTO	Push switch for automatic range selection	Initiates DMM operation to locate range for which the input signal will be measured between 10% and 120% of full scale.

*If function is not included in instrument, switch can not be depressed.

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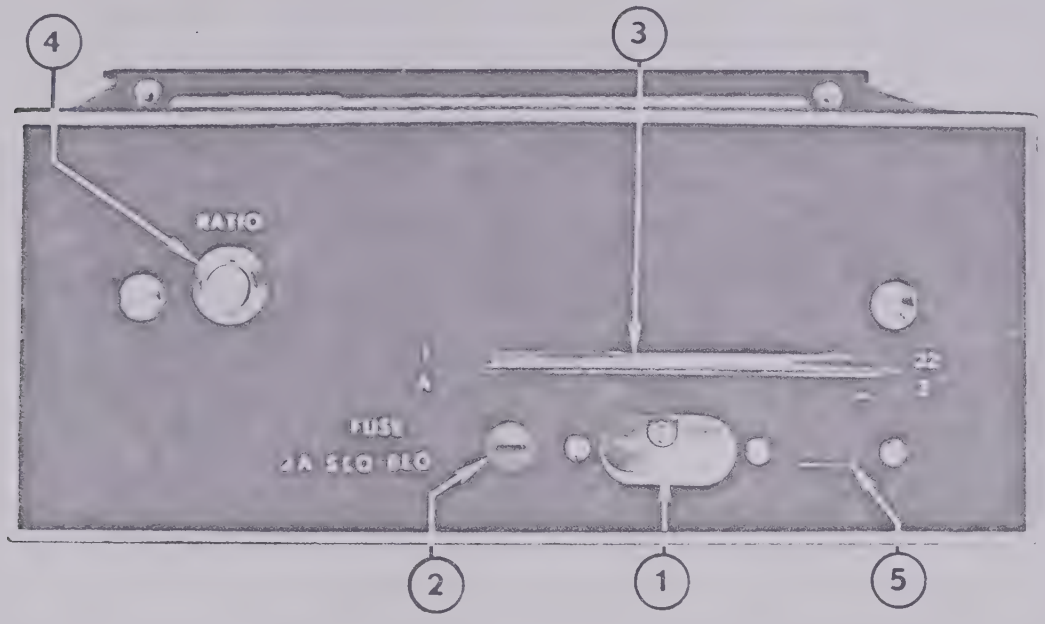

Figure 2-2. MODEL 2500 DMM Rear Panel Controls and Indicators

Table 2-2

REAR PANEL CONTROLS AND INDICATORS

Fig. Ref.	Control/ Indicator	Description	Function
1.	POWER	3-conductor connector	Connector for line cord.
2.	FUSE	Receptacle and holder	For a 2/10 amp slow-blow line fuse.
3.	REMOTE	PC Connector	Provides digital output of measured value, indicates selected range of operation, and provides input for remote control of range and remote triggering of DMM operations.
4.	RATIO	Push-push switch	Selects ratio mode of multimeter operation in which external source is used instead of the internal reference.
5.	LINE VOLTAGE SWITCH	115/230V switch	Connects proper transformer voltage taps so that Series 2000 will work in user area.

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4. a) If using Manual Ranging (paragraph 2.5 a.), select most sensitive range that does not cause DMM to indicate an overrange condition. This will utilize full 5 digits of DMM resolution capability.

b) If using Auto Ranging (paragraph 2.5 b.), wait until display stabilizes at on-scale range before reading.

c. Waveform and Error Comments-AC Mode

In measuring input AC voltages, the DMM circuitry blocks any incoming DC, and the instrument operates within specification accuracy for any superimposed DC voltage up to 500 volts. The DMM measures the average value of one-half cycle of the resulting AC waveform, and calibrates the output display in RMS of an equivalent sine wave.

2.8 VOLTAGE MEASUREMENTS (RATIO)

a. General

Series 2000 DMM will measure the ratio of any AC or DC voltage within normal operating limits referenced to an external DC reference voltage between +1 volt and +11 volts. The displayed ratio value will be 10 times the true ratio.

b. Procedure

1. Press RATIO push button at Rear Panel (Figure 2-2). Observe corresponding lamp lighted on front panel.

2. Select appropriate AC or DC mode. Observe corresponding lamp lighted on front panel.

3. Select appropriate manual range or auto range.

4. Install links as shown in Figure 2-4.

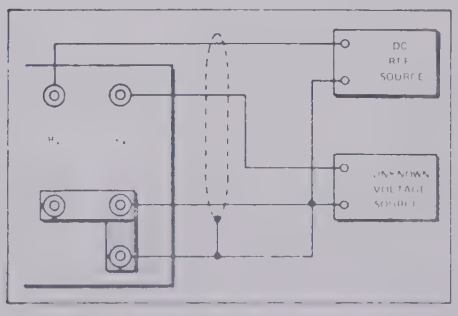

Figure 2-4 DMM Connections for RATIO Measurement

5. Connect voltage input signal to the front panel Vx connectors as in Figure 2-4.

6. Connect the reference voltage input signal to the front panel Rx connectors as shown in Figure 2-4.

7. Read output after display is stable. Divide by 10 to obtain true ratio of unknown to known reference. Sign of display reading will indicate relative polarity of applied voltages for DC inputs.

2.9 RESISTANCE MEASUREMENT

a. General

The Series 2500 DMM measures any resistor between 1.19999 kΩ full scale and 11.9999 megohms full scale and offers full four-wire measurement capability to achieve the specified accuracy. (Series 2400, 1.1999 kΩ - 11.999 megohms full scale.) For rapid measurements, where extreme accuracy is not necessary, the convenience of two-wire resistance measurements is also afforded.

b. Four-Wire Measurements

1. Select kΩ measurement mode. Observe that appropriate lamp is lighted at front panel.

2. Connect the Vx terminals to inner connection points, A, of the unknown resistor as shown in Figure 2-5.

3. Connect the current source and sink to the outer connection points, B, of the unknown resistor as shown in Figure 2-5.

4. Connect GUARD to the low side (current sink) of the circuit as shown in Figure 2-5.

5. Select appropriate manual or auto range switch for expected resistance. Note that highest range of 10000 is available in resistance measurement mode.

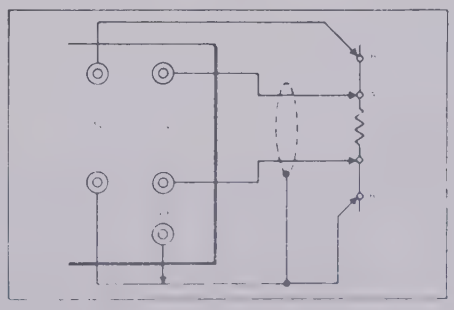

Figure 2-5 Four Wire Resistance Measurement

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6. Observe display. As soon as decimal point location is stable, a correct reading may be made. An over range condition will result in a blinking indication as in voltage measurements (see paragraph 2.5 a.).

7. When measuring high resistance values, it is desirable to shield the resistor through to the connections A and B to reduce the effects of any spurious voltage.

c. Two-Wire Measurements

When making two-wire resistance measurements, connect the unknown resistance and the current source and sink to the connection points as shown in Figure 2-6. Perform the measurement as in steps 4. through 7. in paragraph 2.9 a., above.

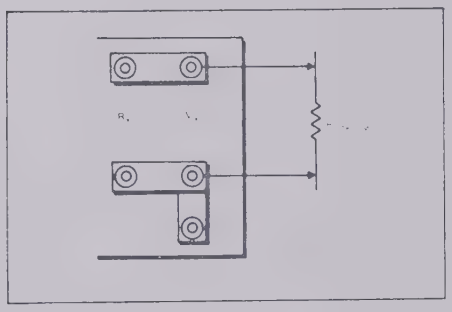

Figure 2-6. Two-Wire Resistance Measurement

2.10 REMOTE OPERATION

a. Set-Up

To obtain remote control and to transmit data from Series 2000 DMM --

1. Prepare a cable with 44-pin connector VIKING 2VK22D/1-3 or equivalent, and cabled as shown in Table 2-3.

2. Remove protective covering from the PC Board connector at Rear Panel and connect cabled connector.

b. Output Signals Specifications and Applications

1. Data Output - Parallel format of five binary-coded decimal digits and sign are transmitted with DTL/T^2L compatibility. Logic is positive true:

Logic "1" +2.4V
Logic "0" +0.4V sink for 4 mA
Polarity positive is logic "1".
Signals remain as latched on output lines between conversions.

2. Range scale in use is indicated by logic "0". Inactive ranges are logic "1"'s.

(Decimal point is indicated by range in use.)

3. End of Conversion (EOC) is indicated by positive going transition of voltage on EOC line, at which time (during transition), the data output is being updated. The negative going voltage transition of the EOC output signal occurs at the start of conversion in each measurement cycle and serves as a forewarning of the positive going transition (and upcoming data update) to occur after 100 milliseconds and within 220 milliseconds thereafter.

4. Overload - A zero logic level on this line indicates the input of a signal more than 120% of the selected full scale range, necessitating a range change. This output thus serves to indicate existence of incorrect data on the output lines and may be used to inhibit input of incorrect data to receiving printers, computers, etc. It also has a short negative pulse at EOC.

c. Remote Control

1. General - In order to exercise external trigger control of Series 2000 DMM, ALL front panel range switches must be placed in the open (non-selected) position.

2. External Trigger - Application of a 2.4V positive voltage pulse between 1 usec and 100 millisec wide causes the instrument to initiate the measurement cycle and to update the data output until the next trigger command. The BCD data remains on the output lines between updates, permitting computer processing or printing (logging), and the repetition rate of the external trigger may be adjusted to allow the necessary time between data updates for data receptors to complete their processing (printing, computer input, editing, etc.).

It is also possible to operate range control remotely and internally trigger:

a) Set range switches to Open.

b) Choose range by grounding proper line.

c) Correct trigger enable (pin J) to external trigger (pin 21) to rear panel.

It is also necessary to select the range to be used by grounding the appropriate line (either logic level or direct ground).

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3. Trigger ENABLE - Logic zero state inhibits conversions when unit is triggered from internal source.

When the level is changed to logic "1" on the ENABLE line, the instrument will make a conversion at the next appearance of a positive pulse or at the next succeeding trigger pulse.

Table 2-3

REMOTE CONTROL/OUTPUT CABLE			
A	Ground	1	Ground
B	$\overline{10^1}$	2	8
C	8,000	3	4
D	4,000	4	2
E	2,000	5	1
F	1,000	6	$\overline{10^4}$
H	$\overline{10^0}$	7	80
J	Enable	8	40
K	NC	9	20
L	NC	10	10
M	NC	11	$\overline{10^3}$
N	800	12	NC
P	400	13	NC
R	200	14	Read Output
S	100	15	80,000
T	$\overline{10^2}$	16	40,000
U	NC	17	20,000
V	NC	18	10,000
W	NC	19	100,000
X	NC	20	+
Y	$\overline{\text{Overload}}$	21	[illegible]
	Ground	22	Ground

Section 3

CALIBRATION

Data Precision 2000 Series Digital Multimeters (DMM) are extremely precise and stable instruments. Their 6-month specified accuracy should last for longer than the specified period. It is advised to check the instrument periodically. When doing so, follow all procedures carefully and observe all precautions.

3.1 CALIBRATION VERIFICATION

Data Precision Company recommends establishing and maintaining a performance history log of the 2000 Series DMM. Transfer the certified factory performance test data as the initial entry. In order to have a locally available test performance for comparison, it is suggested that the instrument be tested against an available standard as soon as it is unpacked and the test results be recorded at that time. The instrument should be checked thereafter at least every six months.

3.2 PRELIMINARY SET UP CONDITIONS

a. Establish a solid ground connection from the case to the power source ground. If the third wire of the three-wire power cord does not carry through to main power ground, ground the meter case with a clip lead attachment.

b. Accuracy of standards used to calibrate the multimeter should be verified before recalibrating the instrument. Errors of standards should be no worse than 20% of the tolerances specified for the multimeter.

3.3 CALIBRATING EQUIPMENT TABLE

The equipment in the table below is recommended for use in the calibration procedure. Substitute units may be employed provided they meet the specified accuracy characteristics.

3.4 ACCESS TO CALIBRATION ADJUSTMENTS

All calibration adjustments are accessible after the top cover has been removed (see Figure 3-1). The actual calibration potentiometers are mounted on the circuit board, but may be reached through an opening provided in the Guard shield. A summary table of Calibration procedure is located on the inside top cover of the instrument.

CAUTION

Do not remove the Guard during Calibration Process.

3.5 CALIBRATING SEQUENCE

Perform the calibration in the following sequence of measurement modes:

1. DC Voltage Measurement Mode
2. Resistance Measurement Mode
3. AC Voltage Measurement Mode
4. Ratio Measurement Mode.

Procedure	Type/Model No.	Performance Specs/Acc. Require.
DC Volts Measurement	COHU/Model 355	10V range ± .001% rdg + 5 uV 100V range ± .001% rdg + 20 uV 1000V range ± .001% rdg + 40 uV
AC Volts	HP/Model 745A and 746A	1mV to 100V: 50Hz-20kHz ± .02% rdg ± .002% range + 10uV 20Hz-100kHz ± .05% rdg ± .005% range ± 50uV 100V to 1000V: 50Hz-20kHz ± .04% rdg 20Hz-50kHz ± .08% rdg
Resistance	JULIE/DMR-105A (.001%) JULIE/XB-106-1M (.0015%) JULIE/XB-107-10M (.003%)	1 kilohm to 10 megohm ± .[illegible] decades

Table of Calibrating Equipment

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Figure 3-1. Series 2000 DMM Interior Showing Access to Adjustments

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3.9 RATIO DC VOLTAGE MEASUREMENT MODE

a. Select DC voltage mode at the front panel and push the RATIO button at the rear panel.

b. Apply full scale (+10V DC) simultaneously to the Vx input and to the Rx input in parallel to front panel.

c. Adjust calibrating potentiometer R86 for a reading of +10.0000.

3.10 POST-CALIBRATION

As calibration is completed, enter date below and initial. Turn off power. Reassemble unit by replacing cover.

CALIBRATION RECORD

Date	Calibrated By (Name)	Date	Calibrated By (Name)

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The analog portion of the TRI-PHASIC A/D converter accomplishes the conversion in the three phases of (1) self zeroing, (2) unknown integration, and (3) reference integration, the latter two compensated by the stored value of compensating offset.

In the Analog Block Diagram (Figure 4-2), one of the three signal conditioning blocks (for Resistance, DC Volts, and AC Volts measurements) is connected via a switching network as the input to the A/D preamplifier. The preamplifier output is integrated and then processed by the high gain amplifier. The high gain amplifier outputs: (1) drive the sign indicator at the end of phase 2 to obtain the switching control signals that select the appropriate polarity of the ISO-Polar™ reference voltage to be applied (via the switching network) to the A/D preamplifier in phase 3 and at the same time drive the Display to indicate sign, and (2) indicate end of phase 3. The high gain amplifier in phase 1 also drives the self zeroing circuitry to develop the offset signal to be applied during the phases 2 and 3 as an input to the A/D preamplifier. Logic and Control

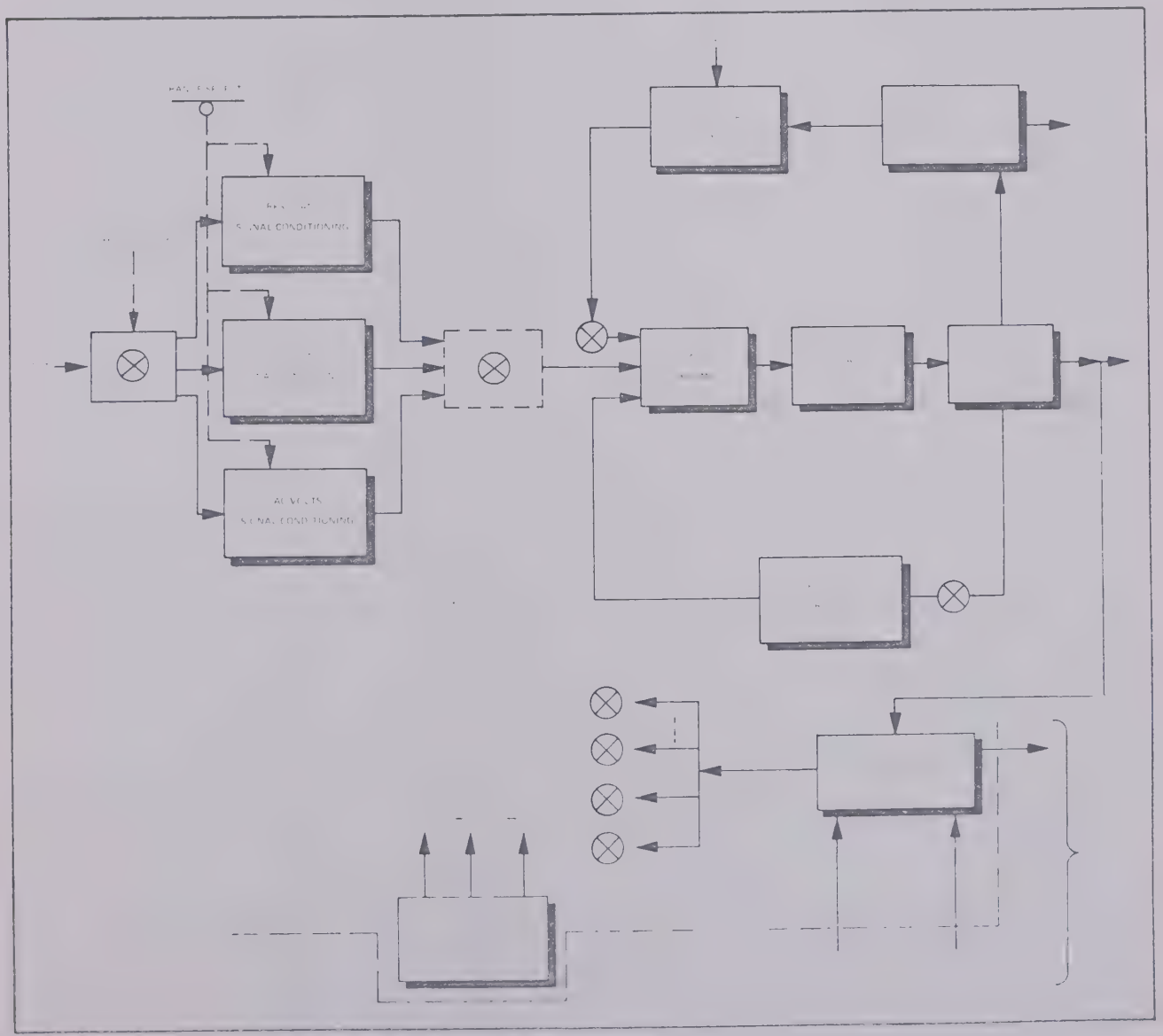

Figure 4-2. DMM Analog Block Diagram

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circuitry in the Analog Block Diagram receive transformer-coupled "trigger" and "start-phase 3" pulses from the Digital Blocks to initiate phase 2 and phase 3 Converter action, respectively, in each conversion cycle and develop end of conversion pulses to be transmitted via transformer coupling to the Digital Blocks to end phase 3. An isolated and triple-shielded Analog Power Supply furnishing ±15V and -5V completes the DMM Analog Block section.

In the Digital Block Diagram (Figure 4-3), the Trigger Block generates a control pulse (from its own internal timing circuitry or from external command) as the "start convert" command to the Enable FF. If not blocked by the External Enable signal, the Enable FF gate permits the Crystal Clock pulses to drive the Decade Counter Chain block to start phase 2 operation. At 100000 counts (end of phase 2) a carry pulse (10^5 CARRY) is transmitted to the Analog Block to start phase 3, while the decade chain continues its counting. When an EOC pulse is received from the Analog Block, the digital control block applies a stop command to the Enable FF stopping the count. At the same time, the Control Block generates a transfer command to enable the transfer from the Counter to the Latches, Decoders, and Drivers, updating the NIXIE™ display. The updated count (at end of conversion) is held in the Latch and the Display until the next update and is also available as BCD output from the Latch Block for remote data output applications.

The Range Select Block is driven by one of three sources: manual range selection, remote range selection, or (when in auto range) a command developed when the range of a particular conversion results in a phase 3 count of less than 10,000 or more than 119,999.

Paragraphs that follow now trace the signal through the functional blocks of Figures 4-1, 4-2, and 4-3.

4.3 SIGNAL CONDITIONING BLOCK

Figure 4-2

An input signal to be measured is introduced into the Signal Conditioning block where it is attenuated according to the range scale chosen, so that a normalized full scale value of ±1.0 volts DC is delivered to the A/D Converter Block. Overrange capability of 120% of full scale is obtained by accurate operation of the Signal Conditioning block to an output value of ±1.2 volts.

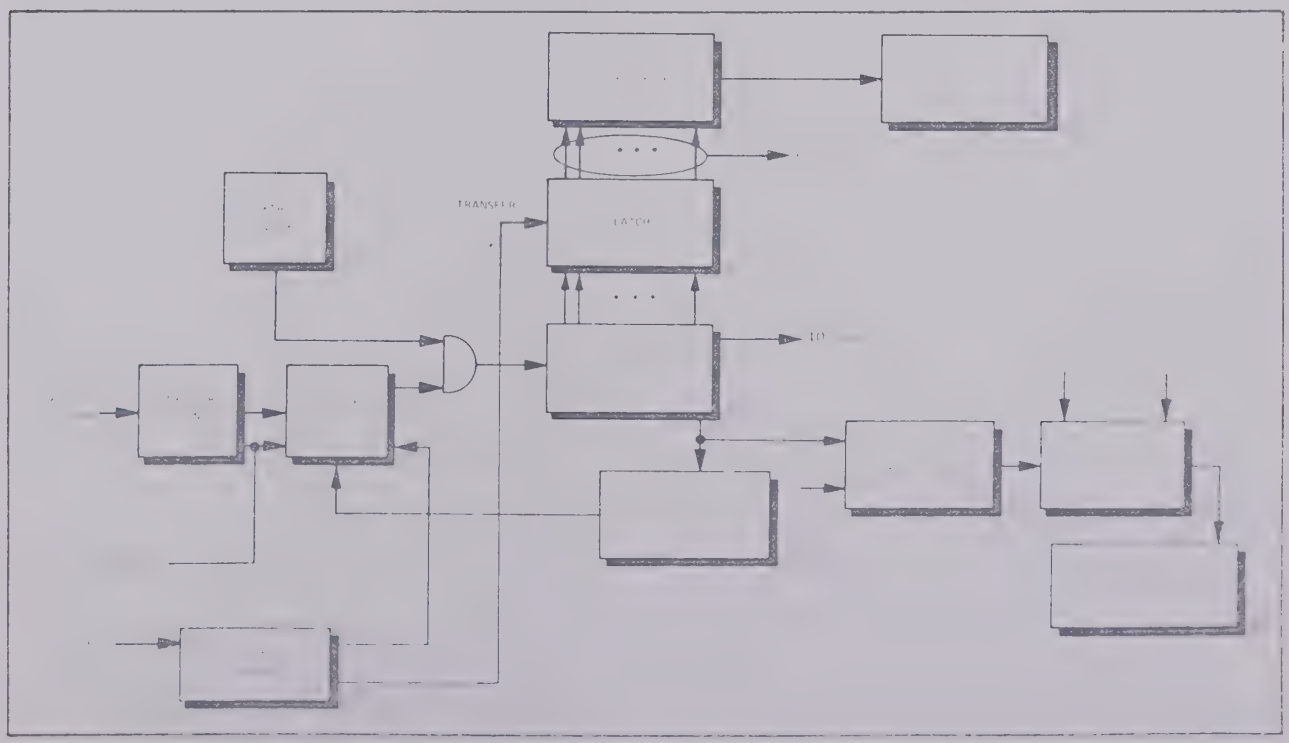

Figure 4-3 DMM Digital Block Diagram

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Signal Conditioning of DC voltage inputs from ±1V to ±1000V full scale is accomplished by inserting appropriate attenuating factors for the selected full scale range. Signal conditioning in the 0.1V full scale (option) range is accomplished in the A/D Converter block.

For AC voltage inputs, the Signal Conditioning block rectifies and filters the input signal so that the output, a DC signal, represents the average value of the sine wave multiplied by the conversion factor of 2.22 to yield the RMS equivalent (Figure 4-4).

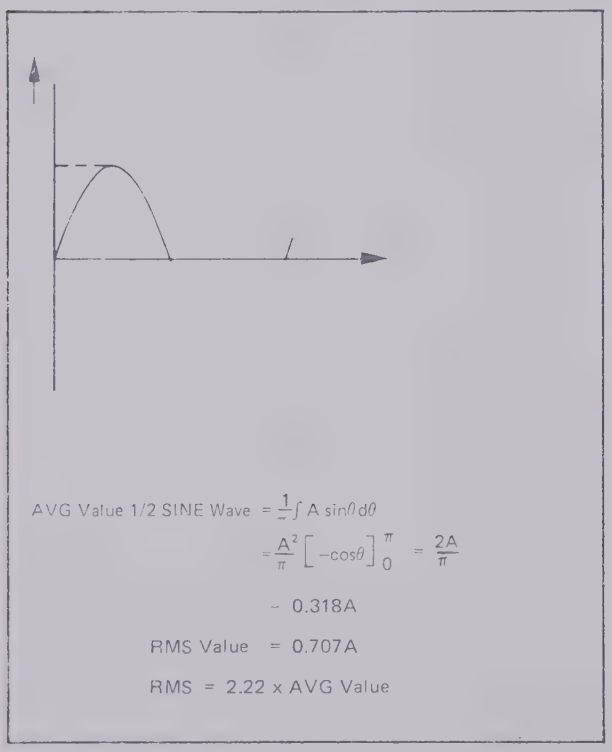
AVG Value 1/2 SINE Wave = $\frac{1}{\pi}\int A \sin\theta d\theta$
$= \frac{A^2}{\pi}\left[-\cos\theta\right]_0^{\pi} = \frac{2A}{\pi}$
= 0.318A
RMS Value = 0.707A
RMS = 2.22 x AVG Value

Figure 4-4. RMS/AVG Scaling Constant

In the Ratiohmic™ resistance measurement technique, a voltage is connected across a range-selected accurately calibrated resistance in series with the unknown resistance, and the voltage drop across the unknown resistance is treated as an unknown DC voltage to be measured as before. In phase 3, however, the voltage drop across the calibrated resistance is used as the reference. Because the unknown and standard resistors are in series, the ratio of voltage drops is a direct measure of unknown resistance.

Attenuation components in the Signal Conditioning block are relay operated in response to control signals. These may be initiated by operating the front panel push buttons at the DMM, by control signals transmitted from a remote station via the rear panel connector, or by control signals generated within the DMM when in AUTO ranging.

4.4 TRI-PHASIC A/D CONVERTER BLOCK (Figure 4-2)

The three pahses of performance of the TRI-PHASIC A/D Converter are:

Phase 1: Accumulation and storage of offset

Phase 2: Integration of Input minus offset

Phase 3: Integration of Reference minus offset

In Phase 1 --

a. Inputs are disconnected from the A/D Converter;

b. Amplifier is clamped;

c. Long-term non-zero offsets are servo-accumulated and stored for later use;

d. Offset is updated continuously until the DMM phase 1 action ends in response to the trigger command.

In Phase 2

a. Clamp is removed and input is connected to the amplifier;

b. Integration of input signal, algebraically reduced by the stored offset value, proceeds for 100 milliseconds as determined by Crystal Clock;

c. Result of the 100-millisecond integration appears as a voltage of the integrating capacitor.

In Phase 3--

a. Input is disconnected from A/D;

b. Voltage of opposite polarity is selected from ISO-Polar reference, algebraically reduced by value of stored offset, and the difference integrated to discharge the integrating capacitor linearly to zero;

c. At the zero crossover, end of conversion is generated, and transmitted to digital control circuitry.

4.5 TRIGGER GENERATOR AND CLOCK (Digital Block Diagram, Figure 4-3)

Primary control for DMM measurement is the trigger which initiates each conversion (start of phase 2). The trigger, in its internal DMM circuitry, is generated by the discharge of a neon tube after an RC path charges a capacitor to the neon tube break-down voltage. The trigger is factory selected for a pulse repetition rate of approximately 3 per second.

The trigger may be blocked and a conversion cycle delayed indefinitely by grounding the ENABLE input for as long a

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desired. The display, or BCD equivalent, is held until a new trigger is generated. In addition, each conversion may be remotely triggered from an external source by a circuit which is activated when all front panel range select push buttons are in the OUT position.

4.6 DECADE COUNTER CHAIN, LATCH, AND DECODER (Digital Block Diagram)

The decade counter chain, latch, and decoder are composed of monolithic IC units (one for each of five decimal digits in each of the counter, latch, and decoder blocks) under control of digital control flip flops.

During phase 2, the counter fills up to 99,999, and the 5th decade carry pulse switches the actions of the Analog block from phase 2 to phase 3 operations.

During phase 3, the counter continues counting until it is stopped by digital control initiated by the EOC (end of conversion) pulse from the A/D Converter block.

The digital control also enables the transfer from decade counter chain to the Latch which acts as an isolating circuit and storage memory. The BCD data are connected to decoder drivers where they activate appropriate decimal lines in the NIXIE tubes.

4.7 RANGING (Digital Block Diagram)

Range scaling is accomplished by relays which may be activated in any one of three ways:

a. Manually - by pushing front panel range select push buttons;

b. Automatically - by digital logic control. When in AUTO Range, if the counter reaches a count of 120000 in phase 3, the AUTO Range control flip flop transmits a level output that selects the highest range possible (according to the DMM model configuration) and for subsequent conversion of less than 10000 counts steps down the selection one range step at a time to the range scale of the maximum resolution;

c. Remotely - when in remote trigger control, a discrete range scale may be selected, by grounding directly, or by a logic low level command.

4.8 POWER SUPPLY BLOCK

The Power Supply block may be connected for either a 115-volt or 230-volt AC Source of frequency from 47 to 420 Hz. The block is essentially two separate sets of supplies, driven from the same input transformer primary. The analog supply is triple shielded, floating, and incorporated in a "guarded" area for proper isolation. It develops ±15V regulated supply voltage for the analog circircuitry, -5V for the digital control in this section, and develops the 6.2 volt, oven controlled, extremely low temperature coefficient, reference source for the A/D Converter. Common ground for the precise reference is used as the high voltage for the isolated digital control section, where the low voltage level is the -5 volts.

The transformer primary drives three additional secondaries whose outputs are rectified and provide +20 volts for relay operation, +180 volts for NIXIE tube operation, and a regulated +5 volts for digital logic. These appear in the digital section of the converter and use the digital ground as their return.

4.9 DETAILED OPERATION

A more complete function diagram of the multimeter is illustrated in Figure 4-5. The major blocks comprising the unit are divided into subunits or are repeated to indicate the several functions performed sequentially by the block, and this division forms a basis for complete systems understanding, detailed circuit explanation, and maintenance. Complete schematics, from which simplified schematics and block diagrams have been derived, are contained in Section 6 and are prepared as fold-outs for convenient reference when reading the following text.

The sequence of functions illustrated in Figure 4-5 consists of the following:

1. Operating mode and Full Scale Range are selected. Proper attenuation elements for the selected range are connected in the Signal Conditioning block.
2. Input signal is applied.
3. Prior to the trigger pulse starting a conversion measurement, the A/D Converter input is clamped, and the Signal Conditioning output is removed from the A/D Converter. During that time, phase 1 drift integration proceeds and the self zeroing circuit determines the A/D amplifier accumulated drift and stores it for phase 2 and phase 3 operation.
4. Following the trigger pulse generated in the Timing & Control unit;
   a) The clamp is removed from the A/D Converter.
   b) The Signal Conditioner Output is connected to the input of the A/D Converter.
   c) The self-zeroed drift is introduced as an algebraic negative offset.

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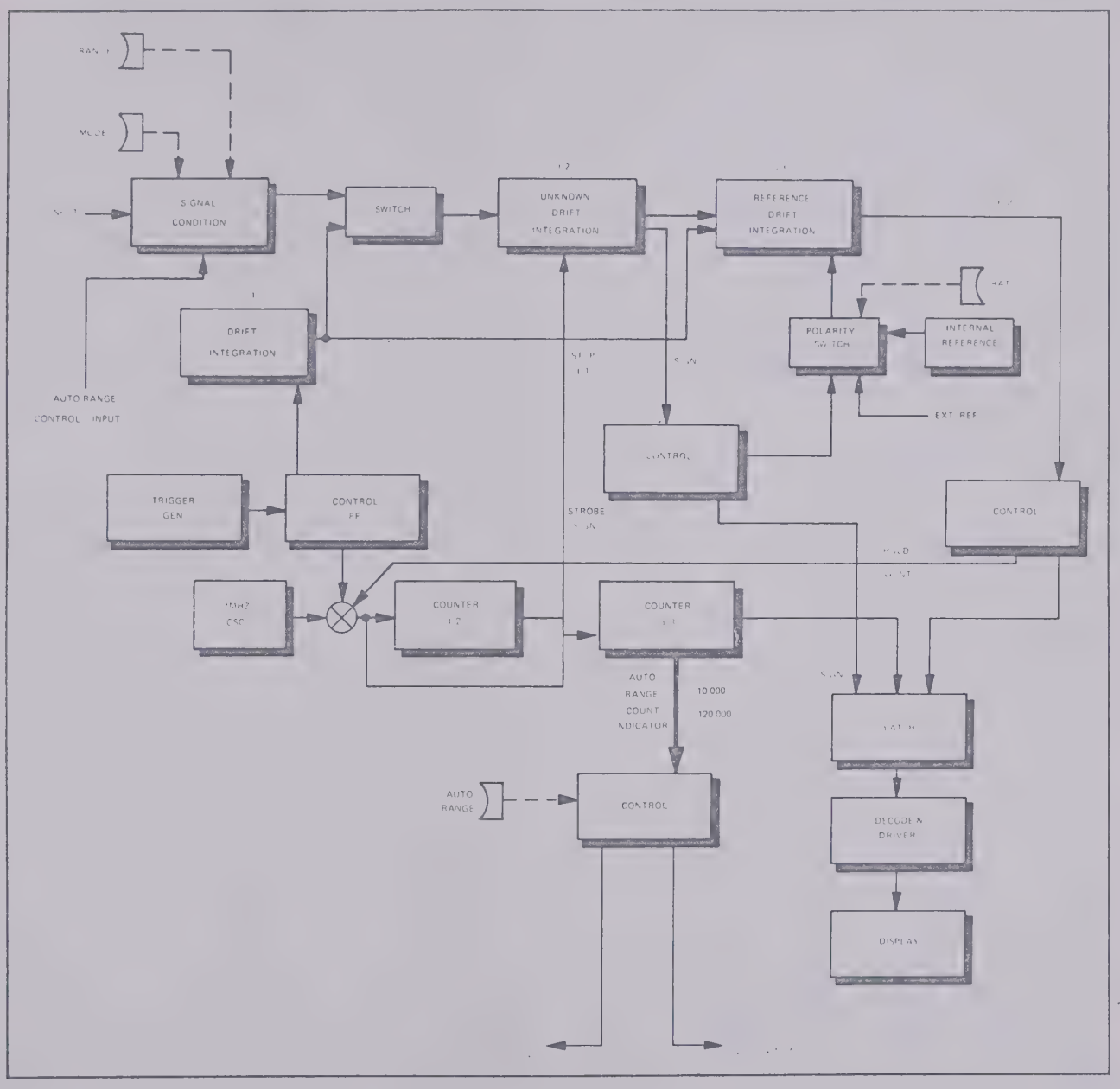

Figure 4-5. DMM Functional System Block Diagram

d) The counter is reset to zero and starts its fixed count for the phase 2 integraton.

5. When the count has reached 100000 (100 millisec.),

a) The second integration is stopped.

b) The sign of the input is interrogated by strobing the integrator output.

c) The unknown signal input is removed from the integrator.

d) The appropriate polarity of internal reference voltage is applied to the A/D input.

e) The reference voltage reduced algebraically by the stored drift (as in phase 2) is integrated during phase 3 integration.

6. When the integrated reference compensates the integrated unknown input (when the output of the integration returns to the starting point),

a) Phase 3 integration process ends.

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b) The input clamp is re-established.

c) The clock input to the counter is stopped.

d) A READ OUT signal is transmitted indicating End of Conversion.

e) The accumulated count is transferred to the display.

The timing sequence is illustrated in the chart of Figure 4-6, indicating the three phases of the operation.

Detailed explanations of these functions are presented in the following sequence:

a. Input signal conditioning.

b. Phase 1 Drift Integration.

c. Phase 2 Unknown-Drift Integration.

d. Phase 3 Reference-Drift Integration.

e. Digital Control and Display.

f. Ranging circuits and Remote display and control functions.

4.10 SIGNAL CONDITIONING DETAILS

a. DC Voltage

Input DC voltages are applied through the HI and LO input terminal, and connected to the input attenuator network through the contacts of Mode Switch S12 and S13 when placed in DC Volts Mode. Relay actions of K1 and K2, determined by the range selection, then establish the attenuator actions.

A simplified schematic of the DC Voltage Signal Conditioning action is shown in Figure 4-7.

The relay pair (K1A and K1B) and relay K2A provide four range selections from 1V Full Scale to 1000V Full Scale. (Range change from 1.0V to 0.1V Full Scale is accomplished in the A/D Converter.) Action of the relays and resultant attenuation of the input signal

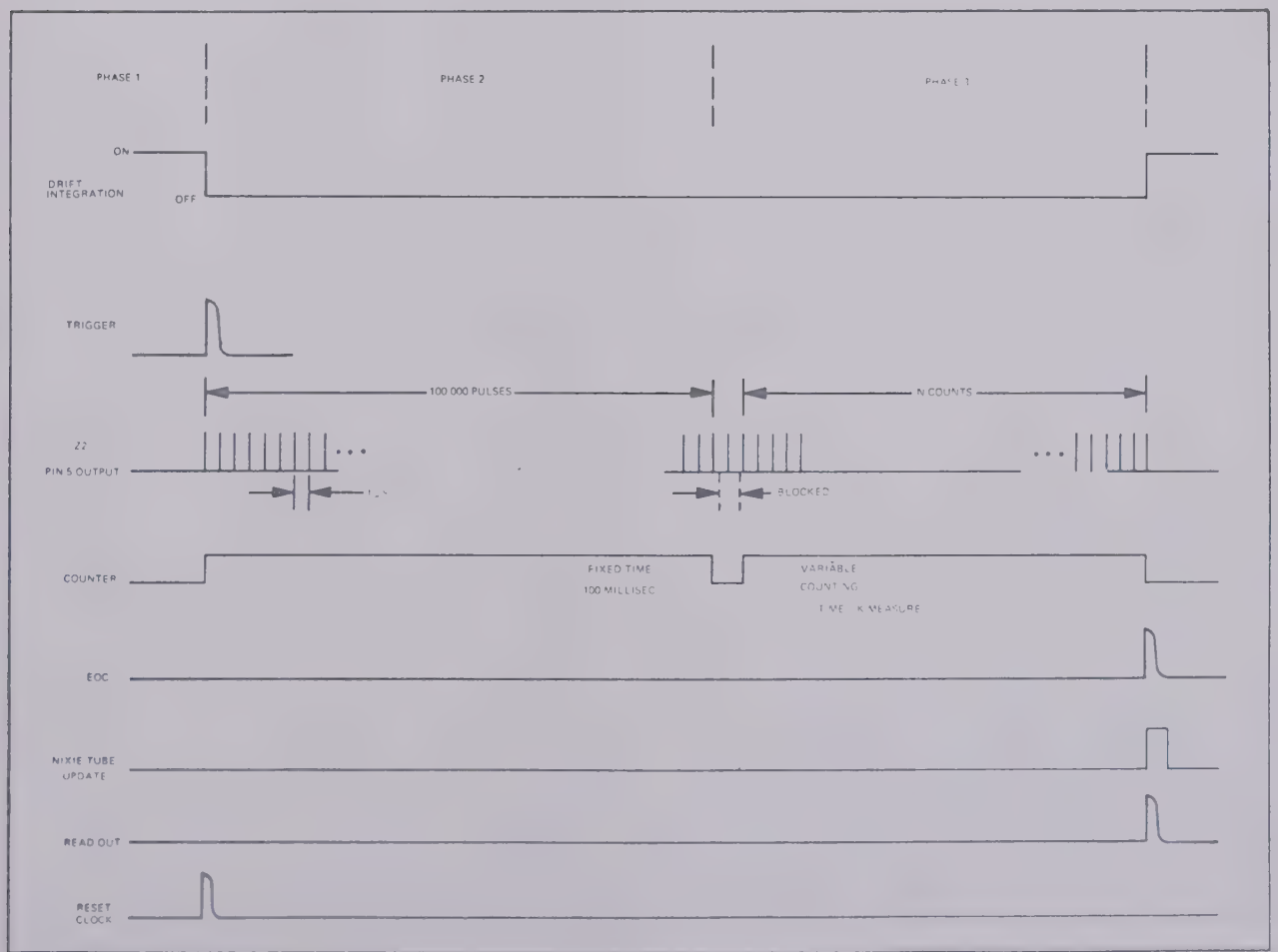

Figure 4-6. DMM System Timing Diagram

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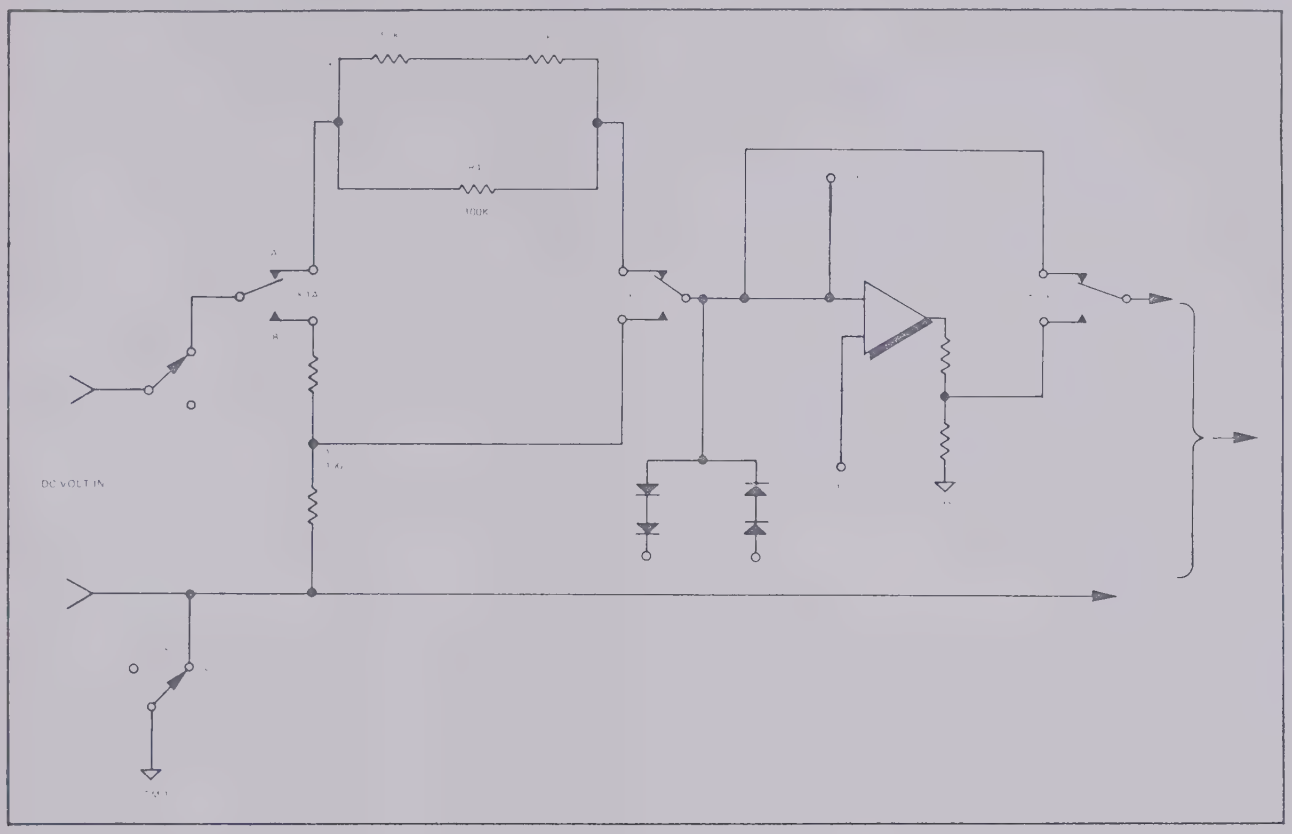

Figure 4-7. DC Voltage Signal Conditioning Simplified Schematic

on the different range scales are summarized by the table below.

Full Scale Range Select.	Relay K1 1/100	Relay K2 1/10	Result. Atten.
1 Volt	OFF	OFF	1
10 Volts	OFF	ON	1/10
100 Volts	ON	OFF	1/100
1000 Volts	ON	ON	1/1000

Full scale voltage delivered to the A/D Converter is 1 volt on all ranges except the 0.1 Volt scale. In that range the full scale output of the Signal Conditioning block is 0.1 volt. In all cases, overrange values, up to 120% of full scale are converted accurately in the A/D Converter, up to a maximum input of 1000 volts DC.

The signal conditioner amplifier is a high impedance, unity gain, isolation unit, provided with voltage and current offset adjustments. It is connected only when relay K2 is activated. The input network, including R41 and the biasing diodes, is designed to protect the Multimeter from accidental connection of high voltages up to ±1000 volts regardless of the range selector setting.

When not in DC Volt Measurement Mode, the input is removed from the indicated circuitry.

b. AC Voltage

In AC Voltage Mode, the input is connected to a broad band active attenuator followed by an active rectifier and filter. Networks in the feedback path of the input amplifier determine the attenuation for the selected full scale range. Capacitor trimmers are adjusted to maintain constant feedback ratios over the range of input signal frequencies. Manual push button action or automatic ranging signals control the relay-operated selection of the appropriate attenuation decade. A simplified schematic of the circuit is shown in Figure 4-8. This illustrates the amplifier and its feedback decades, the half-wave rectification of the second amplifier output, and the low pass filter which passes the average DC component of the rectified output.

The filtered, rectified DC Voltage output is scaled to the RMS value of the applied input signal and feeds the A/D Converter.

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4.12 A/D CONVERTER DETAILS

Operation of the Tri-Phasic A/D Converter in its 3 phases is described with the aid of simplified schematics of Figure 4-10A and Figure 4-10B, derived from the complete reference drawing in Section 6.

Referring to Figure 4-10A, during phase 1, switch Q1 is open, switches Q2, Q23, and Q25 are closed. Opening of Q1 removes the Signal Conditioned input from the A/D preamplifier A1. Closing of Q2 clamps the input to A1, and, with Q23, closes a path whereby C34 is charged from the ISO-Polar reference to 1 volt. Closing of Q25 permits capacitor C36 to store a charge compensating for the accumulated non-zero offset in A1, A2, and Z29.

Appearance of the trigger pulse in the secondary of transformer L2 (Figure 4-10B) signals the start of phase 2, and initiates the control actions by flip flop Z31A. The trigger causes pin 5 to go high and consequently Q1 to close. The output Z31A pin 8 goes low, and consequently opens transistor switches Q2, Q23, and Q25.

a. Opening Q23 opens the charging path to C34 (Figure 4-10A) and leaves C34 charged to 1 volt and isolated during phase 2.

b. Opening Q25 opens the charging path of C36 and leaves it charged with the accumulated compensation for zero drift applied to the input of the differential integrating amplifier A2.

c. Closing Q1 connects the Signal Conditioned output to the A/D Converter input.

Phase 2 integration action takes place in the chain of three active elements: amplifier A1, amplifier A2, and amplifier Z29. Amplifier A1 is a high gain, high input impedance, low offset amplifier whose feedback resistors R93 and R94 determine the closed loop gain.

The output of amplifier A1 is one input to integrating amplifier A2 whose integration constant is determined by C35 and R95. The other input to amplifier A2 is the voltage on C35, the stored value of the voltage compensating for the accumulated zero offset derived in phase 1.

Output of amplifier A2 drives high gain amplifier Z29 to saturation during phase 2. Its output polarity is used to indicate the sign of the unknown input.

Phase 2 integration proceeds until the appearance across the secondary of L4 of a positive-going pulse signalling a 10^5 carry from the digital block. This now appears as a negative pulse clocking flip flop Z30A pin 2 and as a direct set for flip flop Z31A (pin 4). The resulting actions controlled by these flip flops initiate the phase 3 operation of the A/D Converter.

The output, pin 5, of Z31A, which had been high from the start of phase 2, now goes low opening Q1 thereby removing the signal input from the A/D amplifier. Action of flip flop Z30A in response to the clocking pulse depends upon its input conditions just prior to receiving that pulse. This in turn was determined by the output of amplifier Z29 during phase 2. Amplifier Z29 was driven to saturation in the positive or negative direction corresponding to the sign of the input signal.

If the input signal had been positive, Z30A pin 11 would have been low and the clocking pulse would not have changed the high level at pin 6, thus producing no pulse across the primary of "sign" pulse transformer L5. If the input signal had been negative, Z30A pin 11 would have been high and the clocking pulse would cause Z30A pin 6 to go low producing a pulse across the transformer L5 primary and transmitting a negative sign indication to the Digital circuitry. The voltage level developed by flip flop Z30 at pin 9 controls the sign of the reference signal to be switched to the amplifier input at the start of phase 3. (Refer to Figure 4-11 in conjunction with Figure 4-10B.)

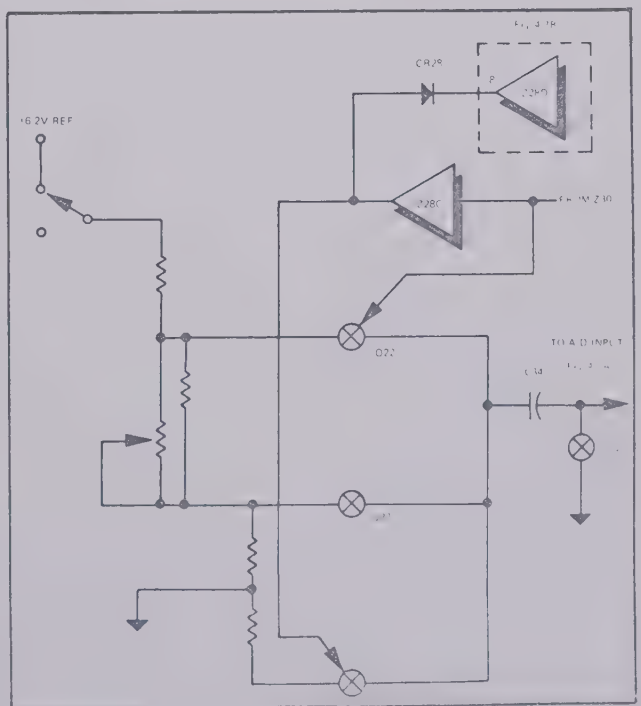

Figure 4-11. ISO-Polar Reference Switching Simplified Schematic

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During phase 2, both Q22 and Q24 are open. The low level output at Z30 pin 9 had kept Q22 open; and the output of Z28 pin 6 had been clamped low through CR28 to Z28D, keeping Q24 open. If the input signal had been positive, Z30 pin 9 would have remained low, keeping Q22 open. The carry pulse control action removes the clamp on the Z28 pin 6 output permitting the output of Z28 pin 6 to go high, closing Q24. This action places the high side of C34 at reference zero potential and negative one volt at the A/D amplifier input. If the input signal had been negative, Z30 pin 9 would go high, closing Q22 and connecting the high side of C34 to reference +2V causing a positive one volt at the A/D amplifier input.

Control actions for the end of conversion (end of phase 3) are initiated by the zero crossing of the Z29 output, sensed by the gating action of Z32C and Z32D, and developed in digital control flip flops Z31. At each gate Z32C and Z32D, two of the three inputs are high during phase 3. As the output of Z29 crosses zero in either direction, one of these gates is enabled and develops the negative direct set pulse at flip flop Z31 pin 10. The Z31D output goes high, is inverted by Z28A, and develops a pulse across EOC transformer primary, signalling end of conversion to the digital circuitry. The Z31D output also controls the resetting of A/D converter to phase 1 operation. It --

a. Closes Q25
b. Closes Q2
c. Clamps Z28 pin 6; opens Q24
d. Direct sets Z30; opens Q22
e. Closes Q23
f. Opens Q1.

In summarizing the actions of the A/D converter circuitry during the three phases of operation, the levels and signals of the gates, flip flops, etc. are tabulated below.

LOGIC LEVELS

ACTION			
INITIAL CONDITIONS Ø1	Z31	1	High
		2	High
		4	High
		5	Low
		6	High
		8	High
		9	Low
		11	High
	Z30	10	Low
		3	High
		6	High
		9	Low
		11	Low
	Q1		Open
	Q2		Closed
	Q22		Open
	Q23		Closed
	Q24		Open
	Q25		Closed
	Z28	8	Low
Ø2 STARTS WITH POSITIVE PULSE THROUGH L2	Z31	1	Clock pulse
		13	Clock pulse
		5	High
		6	Low
		8	Low
		9	High
	Z30	10	High
	Z28	8	Low
	Q1		Closed
	Q2		Open
	Q22		Open
	Q23		Open
	Q24		Open
	Q25		Open
Ø3 STARTS WITH CARRY PULSE THROUGH L4	Z31	4	Neg. pulse
		6	High
		5	Low
	Z30	2	Clock pulse
		3	High if input pos. Low if input neg.
		11	[illegible]
			[illegible] if input pos.
			[illegible] if input [illegible]
			[illegible] input neg.
			[illegible]
			[illegible]

4.13 TRIGGER GENERATOR AND COUNTER

a. Trigger Generation

The trigger pulse initiating each conversion process may originate either from an external source or from internal circuitry shown in the simplified form of Figure 4-12. Capacitor C1 charges toward 180V through R14 until the firing voltage of DS8 is reached. The DS8 neon gap breaks down, and a pulse approximately 100 usec wide and 4 volts magnitude is developed across R16 and connected to the SET ENABLE input of the control flip flop (Z2 pin 2). The sawtooth charge-discharge signal at the junction of R15 and DS8 and resulting trigger timing signal across R16 are also included in Figure 4-12.

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LOGIC LEVELS(cont.)

ACTION	COMP	PIN	LEVEL
	L5		Pulse if input neg. No pulse if input pos.
	Z28	8	High
	Q1		Open
	Q2		Open
	Q22		Closed if input neg. Open if input pos.
	Q23		Open
	Q24		Open if input neg. Closed if input pos.
	Q25		Open
END OF Ø3; Z29 PIN 7 CROSSES ZERO	Z32	6 or 8	Goes neg. pulse
	Z31	10	Low
		8	High
		9	Low

LOGIC LEVELS (Cont.)

ACTION	COMP	PIN	LEVEL
	Z30	10	Low
		6	High
END OF CONVERSION; NEGATIVE PULSE THROUGH L3		9	Low
	Z32	8	High
		6	High
	Z28	8	Low
	Q1		Open
	Q2		Closed
	Q22		Open
	Q23		Closed
	Q24		Open
	Q25		Closed
RETURNING TO Ø1 OPERATION			

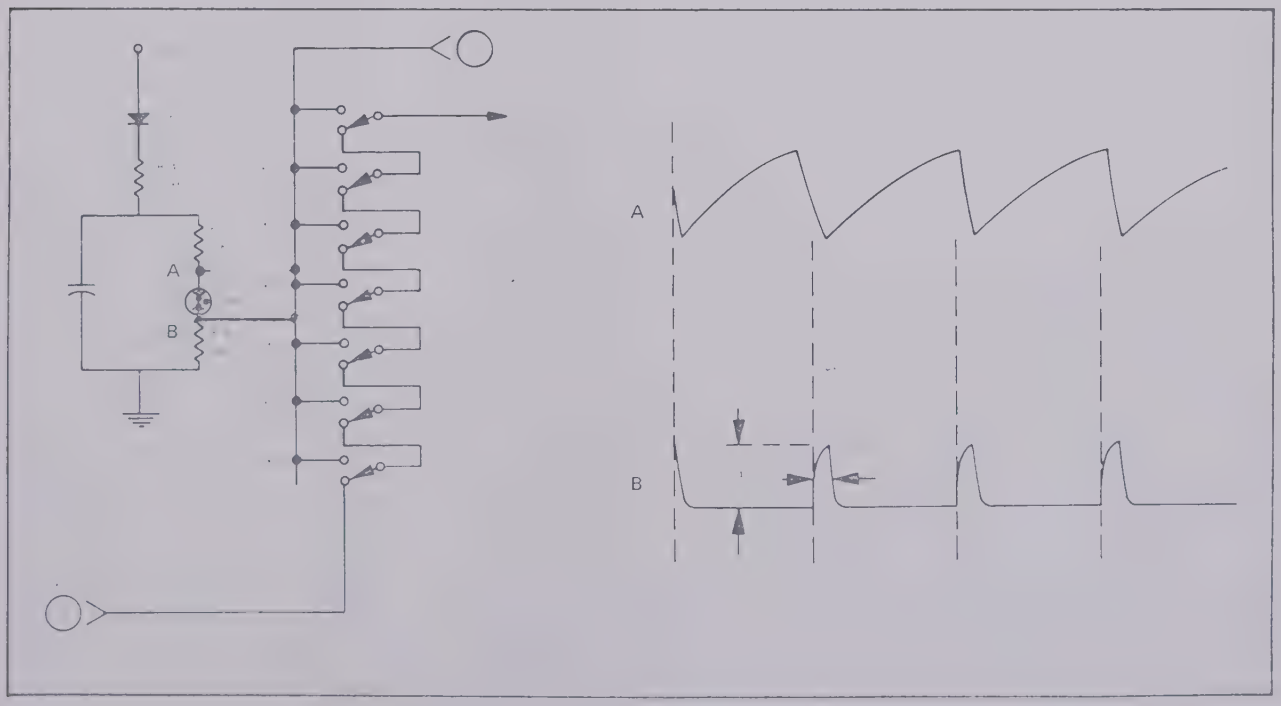

Figure 4-12. Trigger Generator Simplified Schematic and Waveforms

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Non activation of all of the ranging push buttons disconnects this signal (Manual or Automatic) and permits an external trigger pulse to be connected to the DMM flip flop circuitry. If desired, the internal trigger generator may also be used during remote control of the DMM by connecting the output ENABLE of rear panel connector, tab J, to the EXTERNAL TRIGGER input, tab 21.

With the trigger pulse enabling Z2A, the next clock pulse toggles Z2. Pin 5 goes high and pin 6 goes low providing a control output with the following results:

1. After inversion through Z3 pin 3, transistor Q5 conducts; its collector goes low isolating the latching circuit from the counter. The latch and display retain the stored count until the next conversion update, and an output signal, READOUT, is available at the rear panel connector to indicate this event in the cycle. This is a High (T^2L/DTL) output level between conversions.
2. The leading edge of the negative going waveform is differentiated (C5, CR20, and R21) as the input to Z1 (pin 13), inverted, and generates a positive going pulse to reset the decade counter IC's, Z4 through Z8.
3. The inverted counter reset pulse, at the output of Z1 (pin 10) presets the control flip flops Z20 pin 10 and pin 4, and Z2 pin 10.
4. Z3 pin 4 is enabled, allowing the clock to drive the counter.

b. Counter Chain

The crystal-controlled clock is a series-mode crystal circuit consisting of crystal Y1 and inverter Z1. It develops 1 MHz pulses which are gated into the counter during phases 2 and 3. The counter registers accumulate the count during phases 2 and 3 until receipt of the EOC (End of Conversion) pulse at the EOC transformer secondary. This resets flip flop Z2, and pin 5 goes low, blocking the timing pulses at gate Z3 (4, 5, 6). Simultaneously, Z2 pin 6 goes high cutting off Q5, collector voltage goes high, permitting the count in Z4-Z8 and Z2 to be transferred to the latches, and through them to the decoding and display driving registers Z15 and Z19.

Outputs of the counter chain are transferred through the latching registers as BCD data. These are immediately available at the tab connector of the DMM rear panel for remote display or control purposes. In the DMM, the decoding registers Z15 through Z19 convert BCD to decimal signals for their respective NIXIE tubes.

If the DMM is in a manual range selection, and the developed count in phase 3 is less than 120,000, the conversion cycle is complete.

c. Overload

If an end of conversion pulse is not received during phase 3 by the time the counter reaches 120000 (a display of 120000), an OVERLOAD condition exists, and this event is sensed at gate Z3. One input to Z3 (pin 9) is set at a high level by the toggled output of Z20 pin 5 when the count reaches 10^5 in phase 3. When the counter reaches 20000, the second input to Z8 (pin 10) goes high and activates the gate. The gate output, Z3 pin 8 is a negative waveform, available atrear panel connection, pin Y, as an OVERLOAD indicating signal for remote transmission. The overload indicating negative level also is connected at the output of Z1 pin 2 and acts in the same way as the EOC pulse from the Analog Circuitry through Z11 pin 2 as a direct set for flip flop Z2 pin 4.

The overload condition, generating high levels of 10^5 and 2×10^4, back bias CR47 and CR46, respectively, and the combined action cuts off transistor Q2 to turn off the digit indicator (MSD-1) of the most significant digit in display tube DS2. At the start of the next conversion cycle, when the counter is reset, the back bias levels are removed, and the display responds to the 10^5 count to turn DS2 on during the conversion. Thus, the most significant digit blinks as a result of successive overload conditions.

d. Sign

DS1 is the display unit for the sign indication. It is enabled in DC mode only, and is turned on by the action of the sign pulse transformer L5 output via latch flip flops Z14, and strobed into first latch at carry pulse and transferred to second latch at EOC.

4.14 RANGING (Figure 6-4, Drawing 35-1003)

a. Manual Control

All range selections are controlled by the acitons of Relays K1 through K6, and decimal point selection is slaved to the relay acitons. Each relay activation is controlled by a switching transistor (Q12, Q13, Q14, or Q15) driven by its inverter Z24 pins 2, 4, 6, or 8. The truth table included in the reference detail schematic of Section 6 relates the relay actions for each full scale range selection. In manual ranging, grounding the appropriate line via the switch at the front panel, either by grounding the line, or by applying a logical zero at a remote station, operates the required relays via the appropriate inverter, for each selected range.

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Selection of the highest range x 10^4 (for resistance measurement only) biases off all transistor switches Q12 through Q14, and satisfies the truth table conditions for that range.

b. Auto-Ranging

The non-Automatic position of the S/ switch (for Manual Mode) disables the control flip flops Z21 and Z22, A and B, gates Z23, and inverter Z24 (pin 12). The circuitry is enabled when switching to Auto Range, lifting the ground and operating in response to control signals through gates Z21 (pins 3 and 6).

Voltage Auto Ranging

Either of two events causes the Auto Ranging circuit to change its full scale range:

1. An overload indicated by count of 120000 sensed at gate Z21 pin 3;

2. An underrange, indicated by a count under 10000 at end of conversion, sensed at gate Z21 pin 6.

In either event, the gate output is negative going.

Overload

At the overload voltage event, the negative going action of gate Z21 pin 3 acts as a direct set on flip flop Z22A and Z22B. The flip flop outputs apply enabling levels to gate Z23 pins 12 and 13, and cause the output at pin 11 to go low, acting to select the highest voltage range, 10^3.

If the succeeding conversion results in an underrange condition, then, at the READ event, gate Z21 pin 6 is negative going and clocks both flip flops Z22A and Z22B resulting in the stepping of the range selection to the next lower range. The process is repeated, dictated by enabling levels at the flip flops, until the range of maximum resolution for the input signal is selected.

Resistance Measurement Auto Ranging

When in auto ranging during Resistance measurement mode, the mode-switched circuitry disables transistor Q21 and lifts the clamp from flip flop Z21 pins 10 and 11. When an overrange condition is sensed by gate Z21 pin 3, its output causes Z21 pin 11 to go high; then through inverter, Z24, causes pin 12 to go low, producing the same result as closing switch S6A. This action results in the selection of the highest ohms measurement range scale (10^4).

In addition to controlling the relay selection for x 10^4 scale, the action disables flip flops Z22B for the next event by a negative level at pin 2 of flip flop Z22B, and a consequent negative level at pin 12 of Z22A. If an underrange condition should occur at a succeeding conversion, Z21 pin 6 output will not change the states of flip flops Z22A or Z22B. It will, however, set flip flop Z21 pin 8 high and pin 11 low, and through the inverter action of Z24 pin 12 activate Q11 and the x 10^3 range scale select relay. In addition, it will enable flip flop Z22A, and thereby establish the conditions for subsequent toggling response to the next sensing of underrange conditions in the same manner as for voltage measurement auto ranging.

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Section 5
OPERATOR & FIELD MAINTENANCE

5.1 GENERAL

Series 2000 Digital Multimeters use solid state components and integrated circuits (except for display tubes), and are designed for reliable long-life operation. Except for calibration verification, no operator maintenance should be required, and there should be no normal requirement for opening the DMM case. Should any malfunction require corrective action within the warranty period, arrangements should be made to obtain factory assistance.

CAUTION

Data Precision provides this Maintenance Information primarily for users of Series 2000 Digital Multimeters in need of repair after the expiration of the Warranty period. The information is intended for users who are qualified and competent to effect any needed repairs. The equipment may be returned for repairs at a nominal fee if the user should elect to have the factory make repairs.

Should the qualified user attempt to troubleshoot and repair the DMM, he will find that Series 2000 DMM contains a number of features especially designed for simplified unambiguous troubleshooting and fault indication. Among these are:

a. Full and complete design and parts data in this Instruction Manual;

b. A positive troubleshooting procedure intended for effective use by competent technical personnel in isolating and correcting all but the most subtle and intricate problem sources;

c. Mechanical parts layout and identification for logical and easy location.

5.2 PARTS GROUPING AND THE TEST STAND-OFF GRID

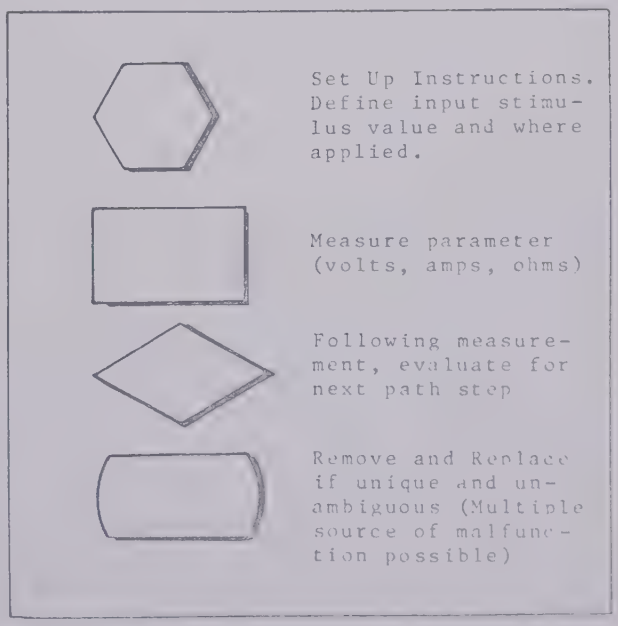
The printed circuit board is etched to show the grouping into major functions of the components (Figure 5-1). These correspond, generally, to the schematics in Section 6. The separate groups are individually named, the designations appearing along the edge of the board. When the Guard is removed, the floating Analog power supply and the analog portion of the A/D Converter and Signal Conditioner are revealed. The two amplifiers of the A/D Converter and the CLAMP/UNCLAMP switching module are separate modular components. They are mounted on the base PC board as integral component assemblies.

Verifying signal values throughout the circuit is considerably simplified mechanically by strategically positioned stand-offs, connected to circuit components for easy access to points where performance may be monitored. Each installed stand-off is identified by an E-number on the schematics, and etched on the PC board. Access to every major critical portion of the circuit has been assured.

5.3 THE TROUBLESHOOTING FLOW CHART

Figure 5-2 is a coded plan for troubleshooting Series 2000 DMM. The chart presents the logical sequence for performing tests so that an interpretation of test results will isolate the circuit components that are functioning properly. The complete sequence then leads the technician to the only components that may be the source of trouble. Signal tracing the isolated faulty circuit group and reference to the schematic for correct values normally will uncover the faulty component.

A standard graphic code has been used in the flow chart:


Set Up Instructions. Define input stimulus value and where applied.
Measure parameter (volts, amps, ohms)
Following measurement, evaluate for next path step
Remove and Replace if unique and unambiguous (Multiple source of malfunction possible)

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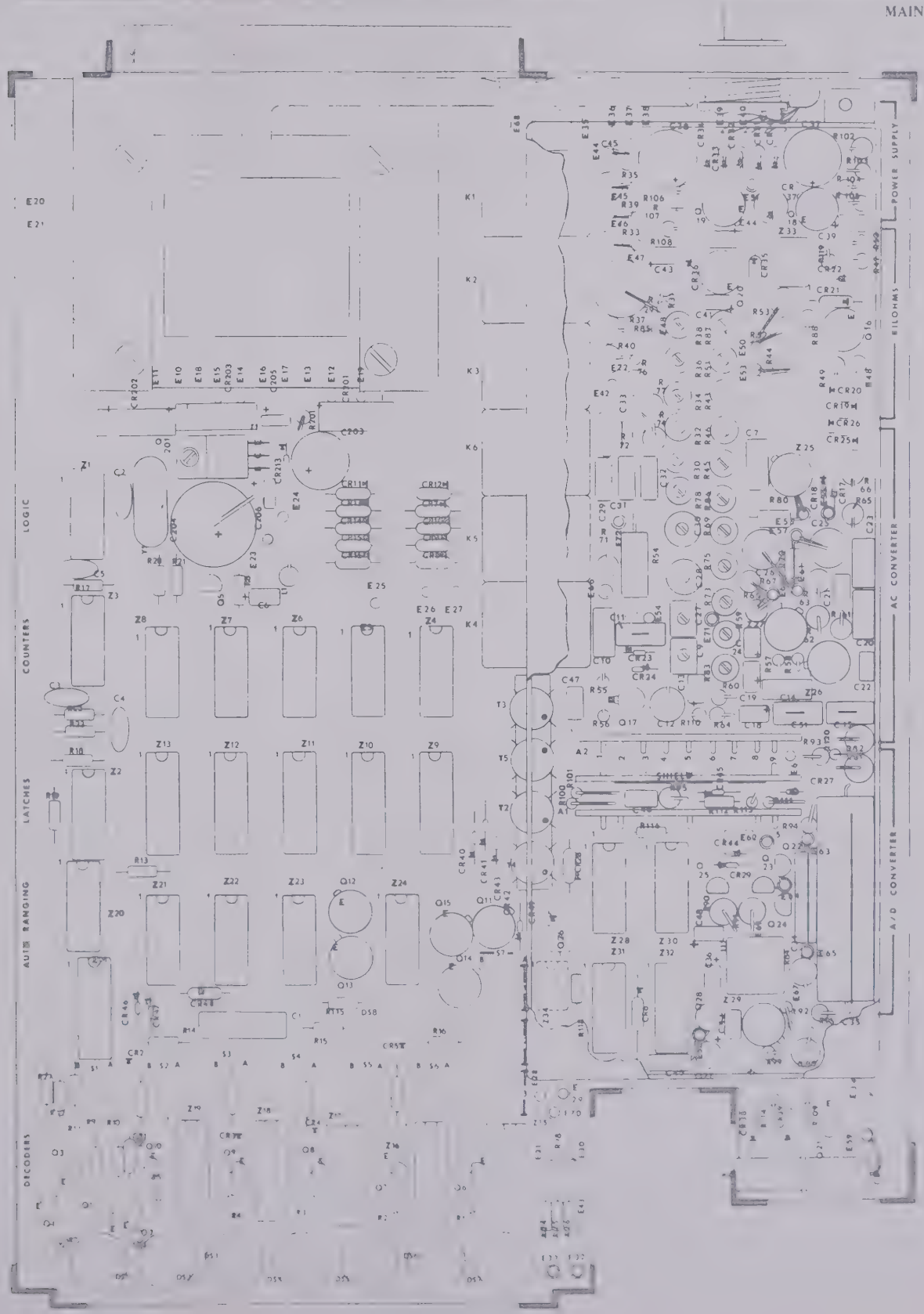

Figure 5-1. Parts and Stand-Off Layout on PC Board Assembly

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The troubleshooting and maintenance procedures are intended for experienced technicians. Use of the flow chart directs the technician to the appropriate circuitry and reference schematic for subsequent detailed component fault isolation, replacement and repair.

5.4 USING THE TROUBLESHOOTING FLOW CHART

As shown in Figure 5-2, one starts by activating the POWER push button and checking to see if the POWER lamp is lit. If not, the chart directs the maintenance man to perform Test No. 1 as as defined in the integral Table of Tests. Test No. 1 calls for the measurement of a DC voltage between stand-offs E18 and E19, and checking for a nominal voltage of +140 volts. If the voltage is present, then, according to the chart, it is concluded that neon display lamp DS13 and its circuitry are in need of further isolation.

If the voltage check of Test No. 1 indicates an incorrect value of the DC voltage, then the chart directs the maintenance technician to use Reference Dwg. 35-1002 and to measure the other output voltages in accordance with Tests 2.1 and 2.2. The Table of Tests also indicates the driven circuits for each of the supply voltages. These may be the cause of incorrect voltage measurements when checking power supply levels and should be checked for excessive current drains by examining driven components and their nearby components for signs of elevated temperatures. The reference drawing includes the pin identification of the components driven by each supply.

Continue through the flow chart as directed, and the successive steps will confirm the proper operation of incremental portions of the DMM as they contribute to the performance as a whole. An incorrect reading in any step identifies the circuit components as a group within which the malfunction most probably originates.

The testing sequence represented by Figure 5-2 is concluded with a calibration to complete the maintenance process. Complete DMM function will have been verified by this process, but only those coded outputs actually tested are verified. Any pattern of missing digits may not be detected in these tests, and such a symptom is indicative of a malfunctioning counter, latch, or decoder IC.

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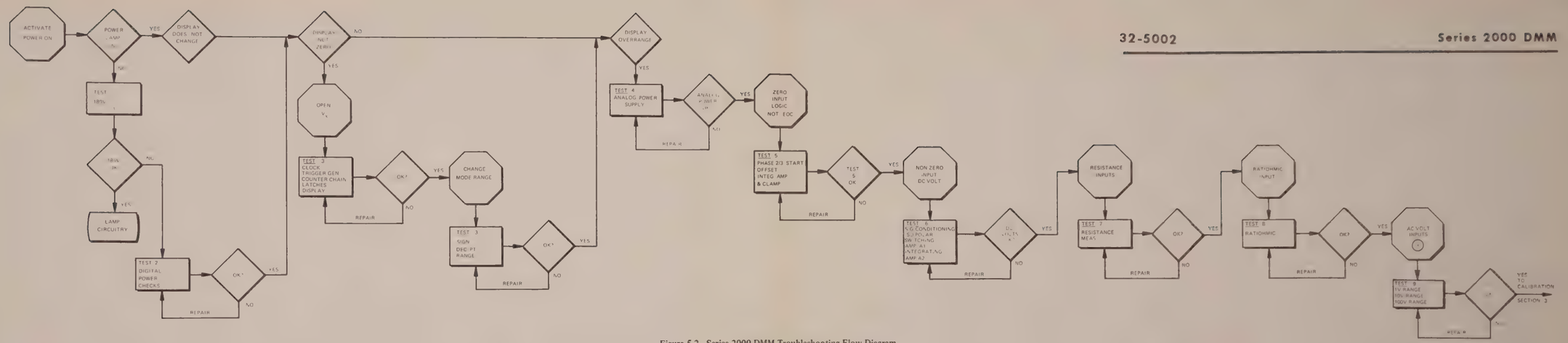
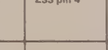


Figure 5-2. Series 2000 DMM Troubleshooting Flow Diagram

TEST NO.	SET-UP	PARAMETER	TEST POINTS	NOMINAL VALUE	LIMITS	IF N.G., CORRECTIVE ACTION REFERENCE	IF O.K., PROPERLY FUNCTIONING SUBSYSTEM
1	Activate Power ON	DC Volts	E18: E19	+140V	+125V to +155V	Power Supply Drawing 35-1002	Neon & Nixie Supply
2.1		DC Volts	E17: E19	+20V	18 to 22	Power Supply Drawing 35-1002	Relay Supply
2.2		DC Volts	E16: E19	+5V	4.5 to 5.5	Power Supply Drawing 35-1002	Digital Logic Supply
3	Open Vx Short Z1A pin 1 to GND						ϕ1, ϕ2, ϕ3; No EOC, 120000 Count
3.1		Frequency Count	Z2A pin 1	1 MHz	±1 kHz	Clock Circuit Drawing 35-1005	Clock
3.2		Waveform Analysis	Rear Conn Pin J	Amp >+2.5V Rep Rate ~3 pps	-0, +5 2.5-3.3	Trigger Gen Drawing 35-1005	Trigger Generator
3.3		Frequency	Z4 through Z8 and Z2 Pin 14 on each	1 MHz to 10 Hz (by 10) and 5 Hz	+ 0.1%	Decade Counter Drawing 35-1005	Decade Counter Chain and Binary Counter
3.4		Logic Levels	Rear Conn DATA OUT Tabs	BCD for 120000		Latches Z9–Z13 Drawing 35-1005	Latch
3.5		Display	Front Panel	120000, Blinking "1"		Display Drawing 35-1005	Display

TEST NO.	SET-UP	PARAMETER	TEST POINTS	NOMINAL VALUE	LIMITS	IF N.G., CORRECTIVE ACTION REFERENCE	IF O.K., PROPERLY FUNCTIONING SUBSYSTEM
3.6	DC V Mode	Sign	Front Panel Display	"+"		Sign Circuit L5, Z14, etc. Drawing 35-1006	Sign Circuit
3.7	AC V Mode	Sign	Display	No Sign		Sign Circuit L5, Z14, etc. Drawing 35-1006	Sign Circuit
3.8	kΩ Mode	Sign	Display	No Sign		Sign Circuit L5, Z14, etc. Drawing 35-1006	Sign Circuit
3.9	No Range Activate	Impedance	Rear Panel Range Tabs 6, 11, T, B, H	Open Ckt		Auto Range Drawing 35-1003	x 10^4 Range
3.10	All Modes a) x 1 b) x 10 c) x 100 d) x 1000 e) x 10000	Display, Relays	Display, Range Relays	Correct Decimal Point Relay per Table		Relay Table Drawing 35-1003	Decimal Point Display Relay Operation
3.11	Auto Range a) DC V b) kΩ c) Jumper Z2 Z2 pin 8 to Z3 pin 8	Decimal Point Decimal Point Value	Display	Decimal Point a) x 1000 b) x 10000 c) "0" x 1		Auto Ranging Drawing 35-1003	Auto Range
4.1		DC Volts	Z33 pin 8	+15V	+ 1V Ripple 1mV RMS	Power Supply Drawing 35-1002	Analog Power Supply

TEST NO.	SET-UP	PARAMETER	TEST POINTS	NOMINAL VALUE	LIMITS	IF N.G., CORRECTIVE ACTION REFERENCE	IF O.K., PROPERLY FUNCTIONING SUBSYSTEM
4.2		DC Volts	Z33 pin 4	−15V	±1V Ripple 1mV RMS	Power Supply Drawing 35-1002	Analog Power Supply
4.3		DC Volts	Z31A pin 7	−5V	±1V Noise 25 μV	Power Supply Drawing 35-1002	Analog Power Supply
5	Short E62 to E71 Jumper Z32A pin 6 to pin 7						Zero Input to A/D No EOC at End of Phase 3
5.1		Waveform	Z31A pin 5	Positive Pulses 100 msec		A/D Conv. Drawing 35-1006	Trigger & 10^5 Carry Start and End Phase 2
5.2		DC Volts	Amp A1 pin 2	200 mV	+0, −	A/D Conv. Drawing 35-1006	A1 Operation OFF SET
5.3		DC Volts	Junction R96, R99	1V	±1V	A/D Conv. Drawing 35-1006	A2 and Clamp Circuits
6	Remove Short Connect Varying Vx DCV ±11V						Supply Varying Input Voltage Values
6.1	DCV Mode Range x 10	DC Volts	E35: E6	Track Input Values (Scope Ind.)		Signal Cond. Drawing 35-1004	DCV Signal Conditioning

TEST NO.	SET-UP	PARAMETER	TEST POINTS	NOMINAL VALUE	LIMITS	IF N.G., CORRECTIVE ACTION REFERENCE	IF O.K., PROPERLY FUNCTIONING SUBSYSTEM
6.2	+10V to Vx Sync. Scope to Z31 pin 5	Waveform	Amp A1 pin 2	+8  -8 100 ms		A/D Conv. Drawing 35-1006	ISO-POLAR Switch Module, Amps A1, EOC Integrating A2
6.3	Reverse Input Vx Polarity	Waveform	Amp A1 pin 2	Reverse Polarity		A/D Conv. Drawing 35-1006	ISO-POLAR Switch Module, Amps A1, EOC Integrating A2
7	Connect for Resistance 2-Wire Connect Resistances in each Range kΩ Mode +	Resistance Measurement	Display	Track Input Value Changes		Signal Cond. Drawing 35-1004	Ohms Converter Signal Conditioning
8	Apply +10V to Both Vx and Rx RATIO Mode 10V Range	Display Count	Display	10.0000	±.1000	Ratiohmic Ckt Drawing 35-1004	Ratiohmic Function
9.1	ACV Mode Range x 1 Apply 11V, 200 Hz	Waveform	Z26 pin 6 CR25, Cathode	1V RMS sin Wave Half-Wave		Signal Cond. Drawing 35-1004	ACV Signal Conditioning
9.2	x 10 Range Apply 10 VRMS 200 Hz	Display Count	Display	Approx. 10		Signal Cond. Drawing 35-1004	ACV Signal Conditioning
9.3	x 100 Range	Display Count	Display	Approx. 100		Signal Cond. Drawing 35-1004	ACV Signal Conditioning

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Section 6

REFERENCE MATERIALS

Section 6 contains reference information in tabular and schematic form.

6.1 Parts Lists

Table 6-1 DMM Assembly
Table 6-2 Amplifier Module A1
Table 6-3 Amplifier Module A2
Table 6-4 Switch Module Assembly
Table 6-5 PC Card Assembly

6.2 Reference Schematics

Figure 6-1 Signal Conditioning Schematic, Dwg. 35-1004
Figure 6-2 A/D Converter Schematic, Dwg. 35-1006
Figure 6-3 Counter and Display Schematic, Dwg. 35-1005
Figure 6-4 Ranging Schematic, Dwg. 35-1003
Figure 6-5 Power Supply Schematic, Dwg. 35-1002

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Table 6-5. PC BOARD ASSEMBLY (Continued)

Circuit Symbol	Description	Part Number
Q16	Transistor MPS6519	14-236519
Q18,20	Transistor 40319	14-2340319
Q19	Transistor 40314	14-2340314
Q22,23	Transistor 2N5246	32-3010-1
Q24,25, 27,28	Transistor 2N5246	32-3010-2
Q201	Transistor 2N5296	14-235296
R1-7	Resistor,15K,10%, 1/2W,CC	12-031538
R8,118	Resistor 2.2K,5%, 1/4W,CC	12-022229
R9-12,27, 109,111	Resistor 10K,5%, 1/4W,CC	12-021039
R13,17, 100,101	Resistor 680 ,5%, 1/4W,CC	12-026819
R15,49, 119	Resistor 1K,5%, 1/4W,CC	12-021029
R16	Resistor 100 ,5%, 1/4W,CC	12-021019
R18,20, 22	Resistor 1.5K,5%, 1/4W,CC	12-021529
R19,21 23,127	Resistor 3.3K,5%, 1/4W,CC	12-023329
R24-26, 79	Resistor 100K,5%, 1/4W,CC	12-021049
R28	Resistor 10M,5%, 1/4W,CC	12-021069
	Resistor Set:	A38-1008-2
R42	Item 1 (9.9M)	
R44	Item 2 (99.75K)	
R43,51	Trimmer 500	12-651007
R45	Trimmer 25K	12-6500
R46,86	Trimmer 100	12-6500
R47,48, 96	Resistor 15K,1%	12-331502
R50	Resistor 261K,1%	12-362613
	Resistor Set:	A38-1007-3
R52	Item 1 (89.75K)	
R52	Item 2 (10K)	
R80	Resistor 47M,5%, 1/4W,CC	12-024769
	Resistor Set:	A38-1007-1
R84	Item 1 (42K)	
R81	Item 2 (10.096K)	
R89	Item 3 (10K)	
R85	Item 4 (37.95K)	
R82	Resistor 1M,1%	12-392003
R83	Trimmer 100K	12-6500
R87	Trimmer 200	12-651005
	Resistor Set:	A38-1007-2
R91	Item 1 (52K)	
R90	Item 2 (10K)	
R92	Resistor 33K,5%, 1/4W,CC	12-023339
R93	Resistor 4.22K,1%	12-334221
R94	Resistor 30.1K,1%	12-333012
R95	Resistor 150K,1%	12-331503
R99	Resistor 3.01K,1%	12-333011
R102	Resistor 1.1K,1%	12-371101
R103	Resistor 8.66K,1%	12-348661
R104,106	Resistor 10K,1%	12-341002

Table 6-5. PC BOARD ASSEMBLY (Continued)

Circuit Symbol	Description	Part Number
R105	Resistor 6.19K,1%	12-346191
R108	Resistor 100 ,5%, 1/2W,CC	12-031019
R112,113	Resistor 20K,5%, 1/4W,CC	12-022039
R114	Resistor 4.7K,5%, 1/4W,CC	12-024729
R116	Resistor 100M,10%, 1/4W,CC	12-021078
R120	Resistor 1M,5%, 1/4W,CC	12-021059
R201	Resistor 1K,5%, 1/2W,CC	12-031029
S1-7	Switch	A38-1010
T2-5	Transformer,Pulse	B38-1005
U1	Assembly Switch Module	PL30-1003
Y1	Crystal 1MHz	A38-1012
Z1,24,28	IC 9937	14-319937
Z2,20, 22,31	IC 9094	14-319094
Z3,21,23	IC 9949	14-219949
Z4-8	IC 7490	14-337490
Z9-14	IC 7475	14-337475
Z15-19	IC 7441	14-337441
Z25	IC LM308	A32-3009
Z29	IC LM311	14-300311
Z30	IC 9945	14-319945
Z32	IC 9962	14-319962
Z33	IC N5558U	14-305558

Table 6-5A. PC BOARD ASSY OPTIONS

Circuit Symbol	Description	Part Number
C8	Capacitor .15uF,600V, PolySty	13-510004
C9,27	Capacitor 2-9pF	13-800002
C10	Capacitor 10pF,520V, DM10	13-310002
C11	Capacitor 10pF,1KV	
C12,25, 26	Capacitor 1uF,50V, PolyC	13-510001
C13,18, 19	Capacitor 5.6uF,20V	13-411030
C14	Capacitor 150pF,DM15	13-311015
C15	Capacitor 20pF,DM10	13-210006
C20,23	Capacitor 5pF,DM10	13-310001
C28,30	Capacitor 15-60pF	13-810001
C29	Capacitor 100pF,DM15	13-311011
C32	Capacitor 1200pF,DM15	13-311037
CR23-26	Diode 1N4148	14-110001
Q17	Transistor	38-1004
	Resistor Set:	A38-1006
R29	Item 1 (6429)	
R33	Item 2 (61.875K)	
R35	Item 3 (618.75K)	
R30	Trimmer 25K	12-651014
R31	Resistor 162K,1%,60C	12-400001

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Table 6-5A. PC BOARD ASSY OPTIONS (Continued)

Circuit Symbol	Description	Part Number
R32	Trimmer 250	12-651006
R34	Trimmer 2.5K	12-651010
R36	Trimmer 500	12-650007
	Resistor Set:	A38-1007-3
R37	Item 1 (89.75K)	
R40	Item 2 (10K)	
R38	Trimmer 25K	12-650014
R39	Resistor 6.19M,.1%,60E	12-400002
	Resistor Set:	A38-1008-1
R54	Item 1 (1M)	
R71	Item 2 (1M)	
R72	Item 3 (110K)	
R62,63,74	Item 4 (10K)	
R76	Item 5 (1.1K)	
R61	Item 6 (1.69K)	
R65,66	Item 7 (2.49K)	
R67	Item 8 (301K)	
R68	Item 9 (178K)	
R55,56, 57	Resistor 39K,5%, 1/4W,CC	12-023939
R58	Resistor 8.2M,5%, 1/4W,CC	12-028259
R59	Trimmer 100K	12-650016
R60	Resistor 150K,1%,55D	12-331503
R64	Resistor 100 ,1%,60D	12-361000
R69	Trimmer 5K	12-650011
R70	Resistor 100K,5%, 1/4W,CC	12-021049
R73,78	Trimmer 2.5K	12-650010
R75	Trimmer 250	12-650006
R77	Resistor 10K,1%,55C	12-341002
R110	Resistor 1K,5%, 1/4W,CC	12-021029
Z26	IC LM301A	14-300301
Z27	IC 7715	14-307715

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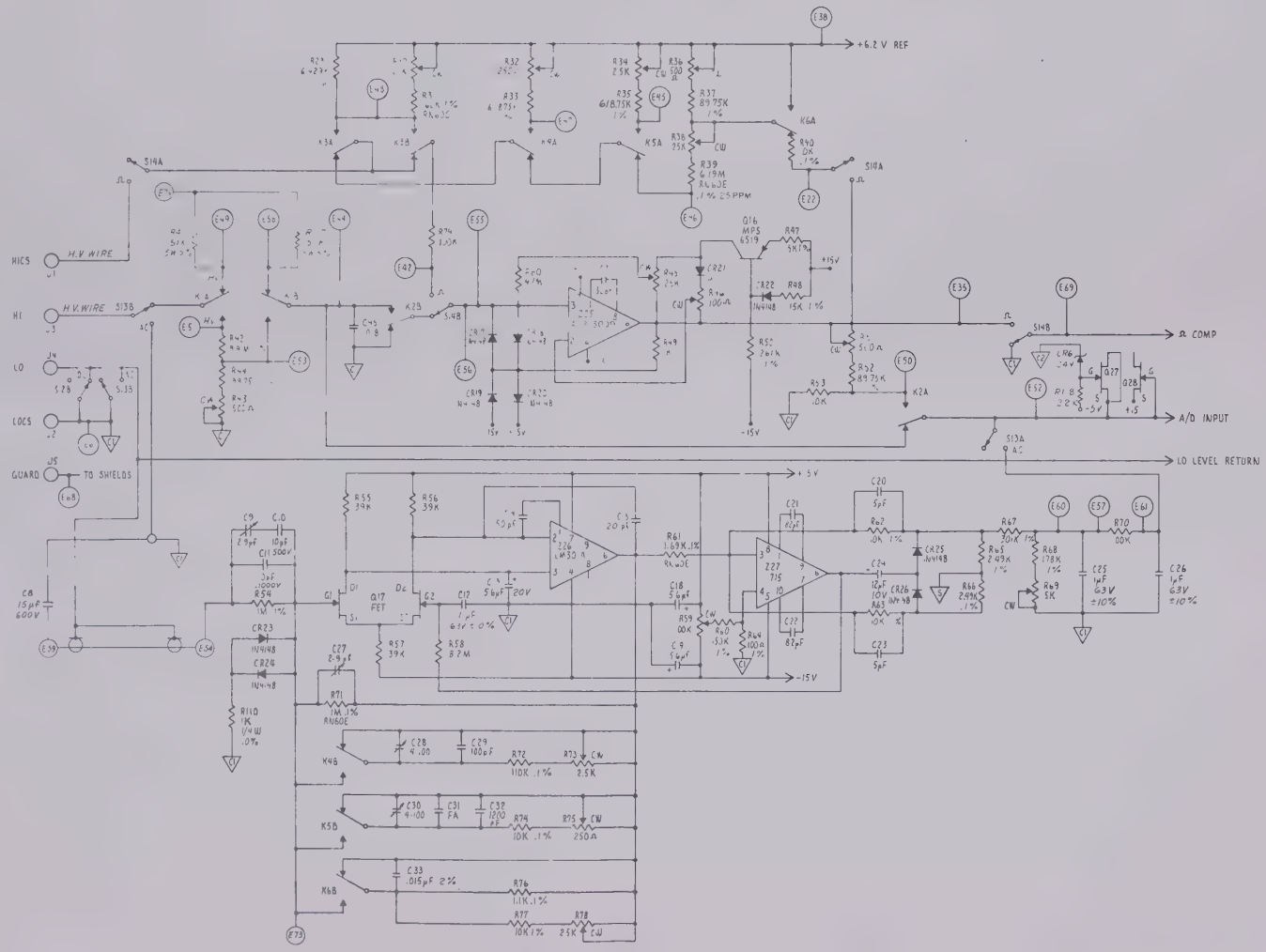

Figure 6-1 Signal Conditioning Schematic Dwg 35 1004

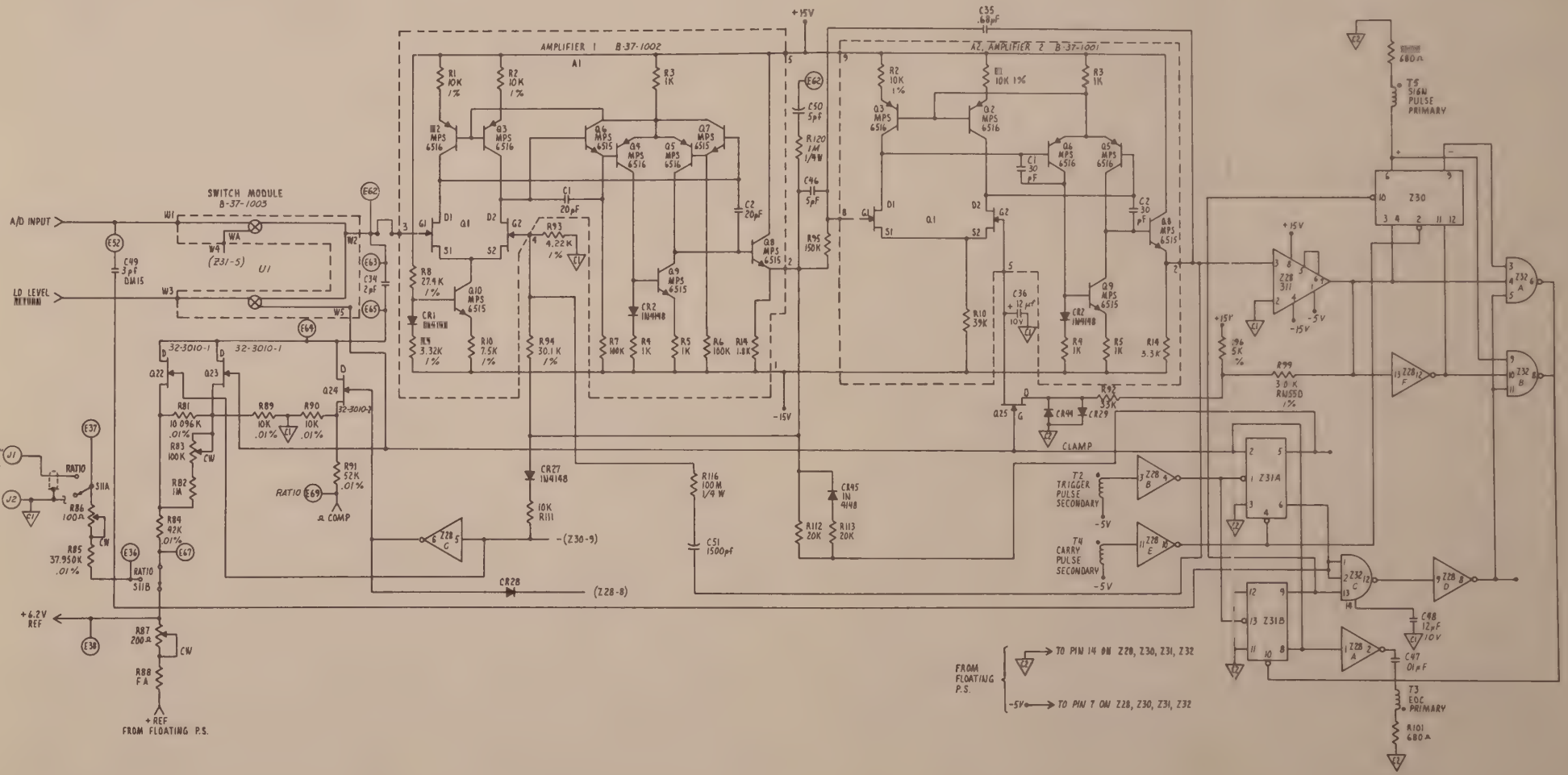

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Figure 8-2. A/D Converter Schematic, Dwg. 35-1006

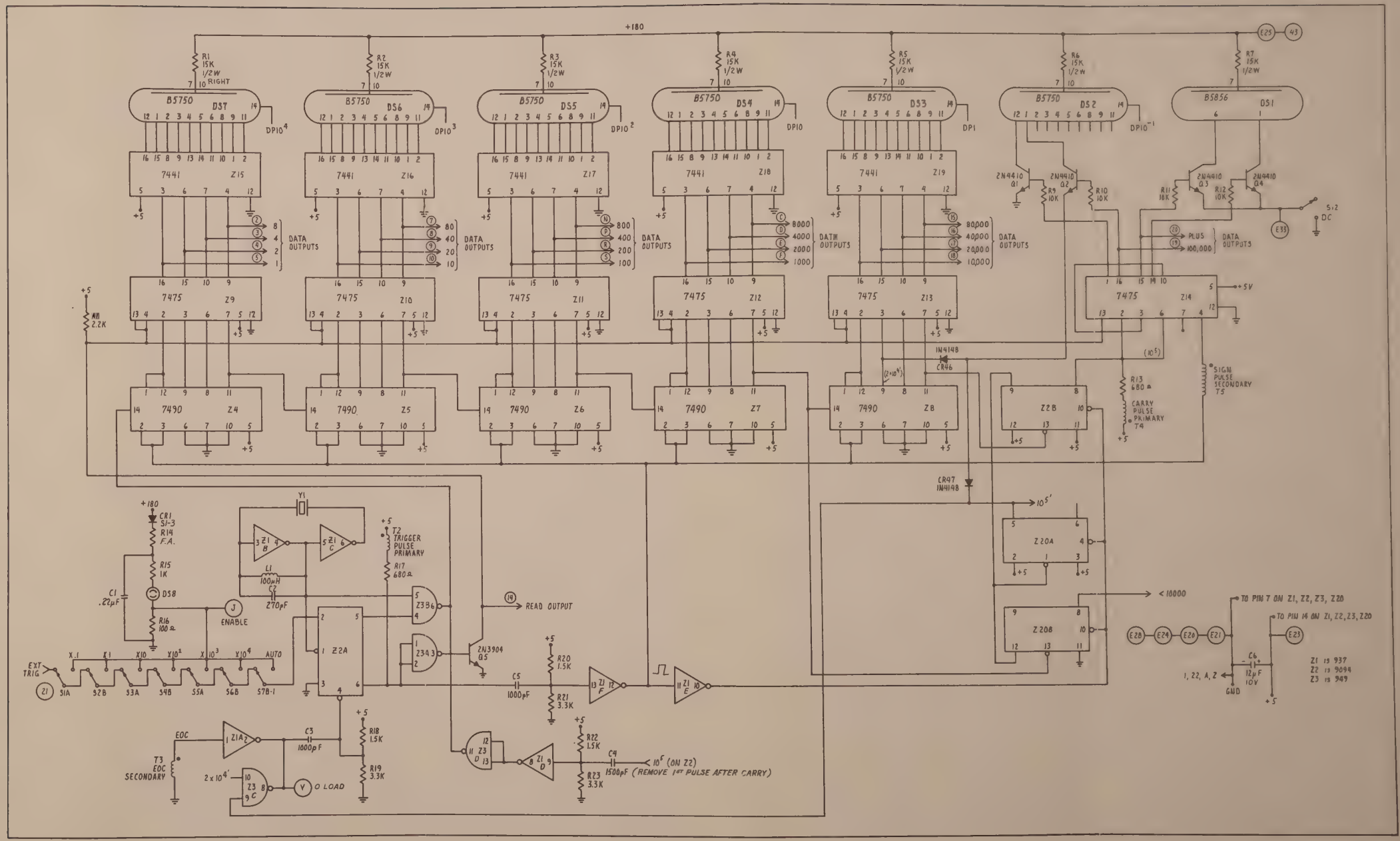

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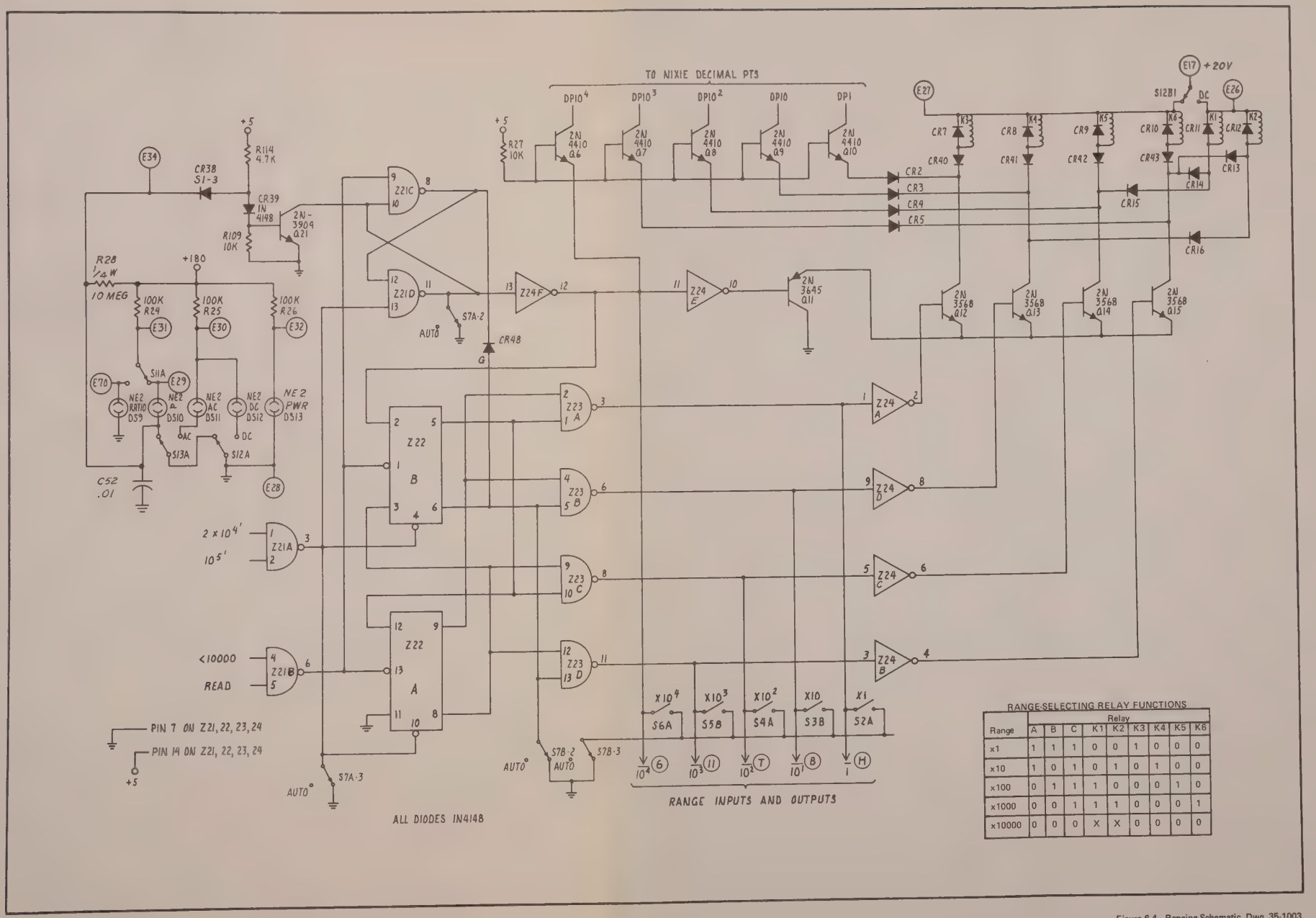
Figure 6-3. Counter and Display Schematic, Dwg. 35-1005



RANGE-SELECTING RELAY FUNCTIONS

Range	Relay								
	A	B	C	K1	K2	K3	K4	K5	K6
x1	1	1	1	0	0	1	0	0	0
x10	1	0	1	0	1	0	1	0	0
x100	0	1	1	1	0	0	0	1	0
x1000	0	0	1	1	1	0	0	0	1
x10000	0	0	0	X	X	0	0	0	0

Figure 6-4. Ranging Schematic, Dwg. 35-1003

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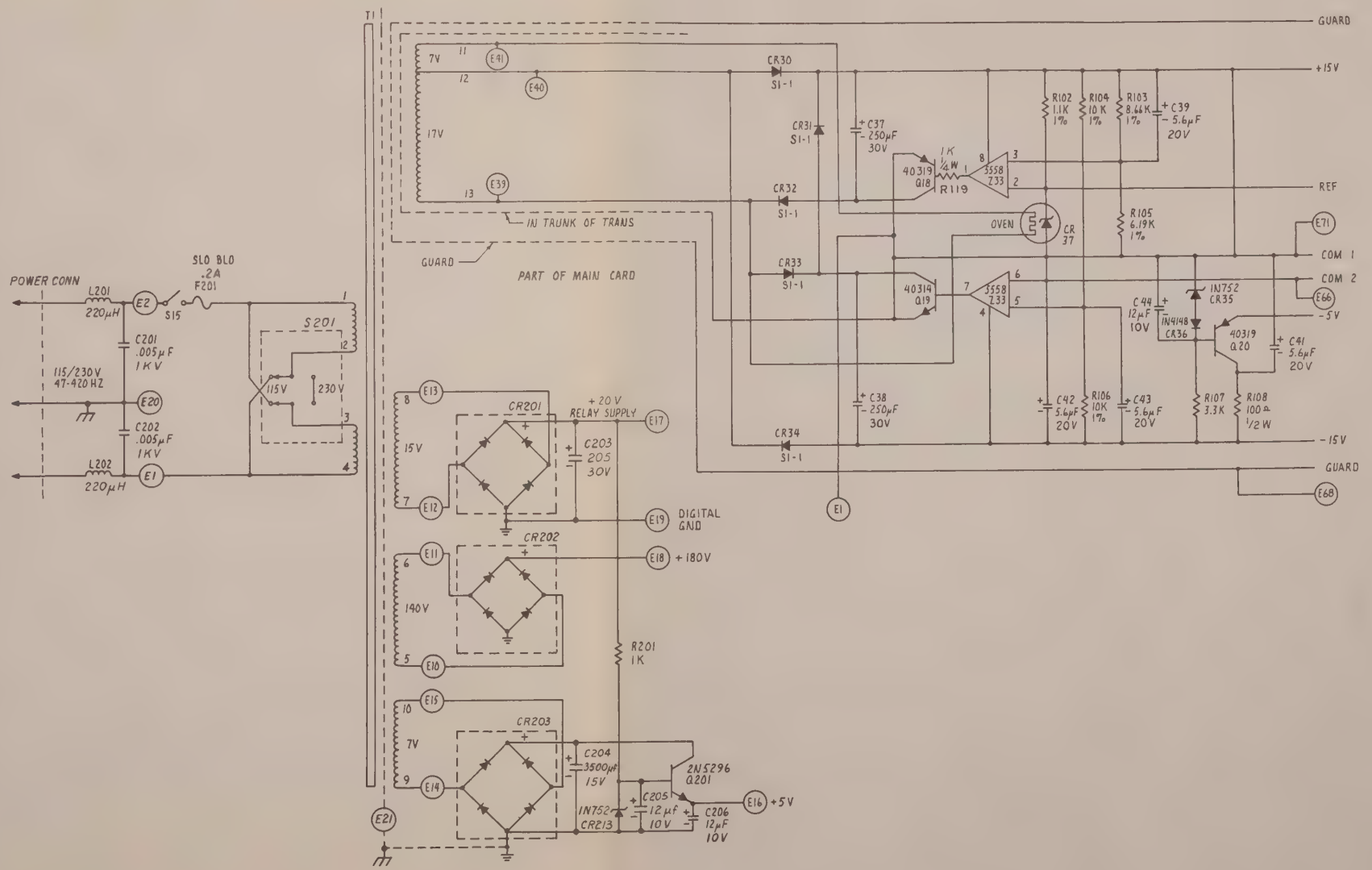

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Figure 6-5. Power Supply Schematic, Dwg. 35-1002

A1 OPTION for MODEL 2500 (Low Level Option)

GENERAL

This A1 Option provides the user with a manually selected 0.1V range as a direct reading display of the Model 2500 multimeter for DC voltage readings. This 3-page supplement describes the circuit changes, the theory of operation, calibrating procedures, and includes schematics of the circuit modifications. The modified schematics are identified with the same basic figure number as appears in the manual.

FUNCTIONAL OPERATION (Refer to para 4.10, 4.12, and 4.14)

The 0.1V range display is accomplished by changing the resistors in the feedback path of the A/D converter amplifier so that the gain during the integration of the unknown signal input integration is 10 times that during the reference integration. The signal conditioning configuration for the 1-volt scale is used during 0.1V range operation, and the decimal point has been shifted one decade to the left. The resulting displayed count will be direct reading for .1V (or 100mV) full scale.

Remote operation of the decimal point is accomplished by grounding the appropriate line for the 0.1V scale at the rear connector.

DETAILED OPERATION

a. Display (See Ranging Logic Modification, Figure 6-4A)

The 0.1V range is chosen by pushing front panel button marked ".1". This action closes S1B, completing the circuit from emitter Q31 to ground, thereby operating the 0.1 decimal point indication. Grounding S1B also grounds pin X on the rear connector for remote 0.1 decimal point indication. For remote control, externally grounding pin 5 results in 0.1V range operation when all front panel buttons are in the open, released, position.

b. Tri-Phasic A/D Converter (See A/D Converter Modification, Figure 4-10C)

When the 0.1V range is selected the A/D Converter gain is controlled during the three phases of the conversion cycle by the FET switches according to the tabular listing below. The revised schematic of figure 4-10C shows the location of the switches and their effect on the circuit.

	Q1	Q2	Q3	Q4
During Phase 1 (Auto-Zero).	OPEN	CLOSED	CLOSED	CLOSED
During Phase 2 (Integrate Unknown)	CLOSED	OPEN	CLOSED	OPEN
During Phase 3 (Integrate Ref)	OPEN	OPEN	OPEN	CLOSED

The resistor components R9, R10, R15 are factory selected so that R10 is exactly nine time R15, and as a result, the gain of the buffer amplifier stage during phase 2 is 10 times the gain during phase 3. During phase 2 the integrator capacitor stores 10 times as much charge as would otherwise be discharged during phase 3. (Therefore, when in 0.1V full scale, the count will take ten times as long as on the 1 volt scale.) Because the decimal point has been positioned one decade to the left of the one volt scale location, the resulting display is direct reading for 0.1V full scale.

CALIBRATION

Calibration of Series 2500 DMM with A1 Option in the DC Voltage Measurement Mode is detailed in this supplement as paragraph 3.6.A. It replaces paragraph 3.6 of the basic manual. All other calibrating procedures remain unchanged.

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3.6A DC VOLTAGE MEASUREMENT MODE, MODEL 2500/A1

Depress "ON" switch; wait one hour for calibration.

a. Zero Adjust: R45, R46

1. Select DC Volts Mode
2. Set range to .1V Full Scale
3. Connect shorting bar across input, Vx
4. Adjust R300 for ± 0.00000 display value
5. Set range to 10V Full Scale
6. Connect (approx.) 10 megohm resistance across input Vx
7. Adjust R45 for ±0.00000 display value
8. Connect shorting bar across input Vx
9. Adjust R46 for ±0.00000 display value
10. Repeat steps 6 through 10 as necessary

b. Balance Adjust: R83

1. Set Range to 1V Full Scale
2. Apply approximately 1V to input Vx
3. Read display. Record
4. Reverse input polarity. Record. Compare with step 3. above
5. Adjust R83 until values of 3. and 4. are exactly same on display
6. Repeat steps 3. through 5. as necessary

c. Reading Adjustments

For each full scale range, apply positive full scale voltage and adjust the appropriate potentiometer for full scale value on the display.

Set F.S. Range to	Adjust	For Reading of
1) 1-Volt Range	R87	+1.00000
2) .1-Volt Range	R17	+0.10000
3) 10-Volt Range	R51	+10.0000
4) 100-Volt Range	R43	+100.000

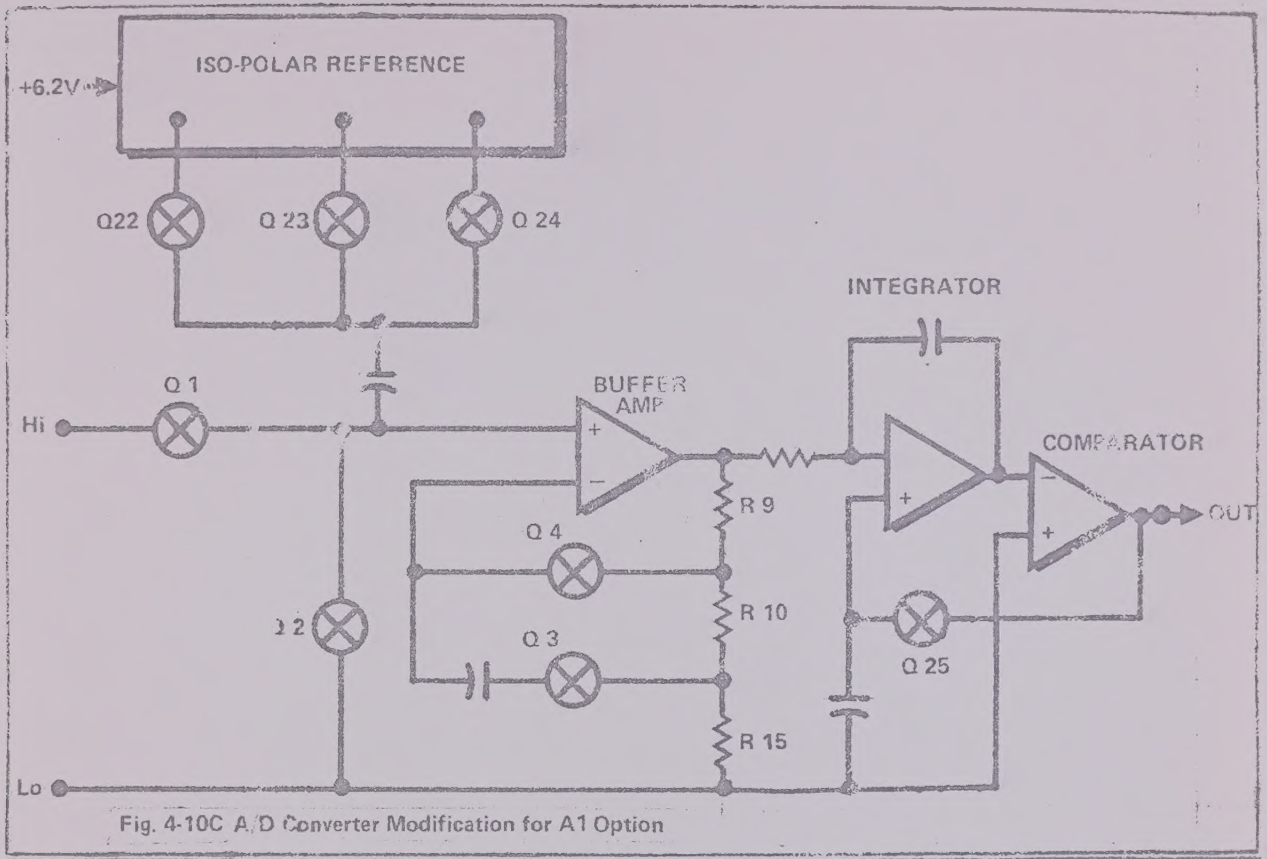

Fig. 4-10C A/D Converter Modification for A1 Option

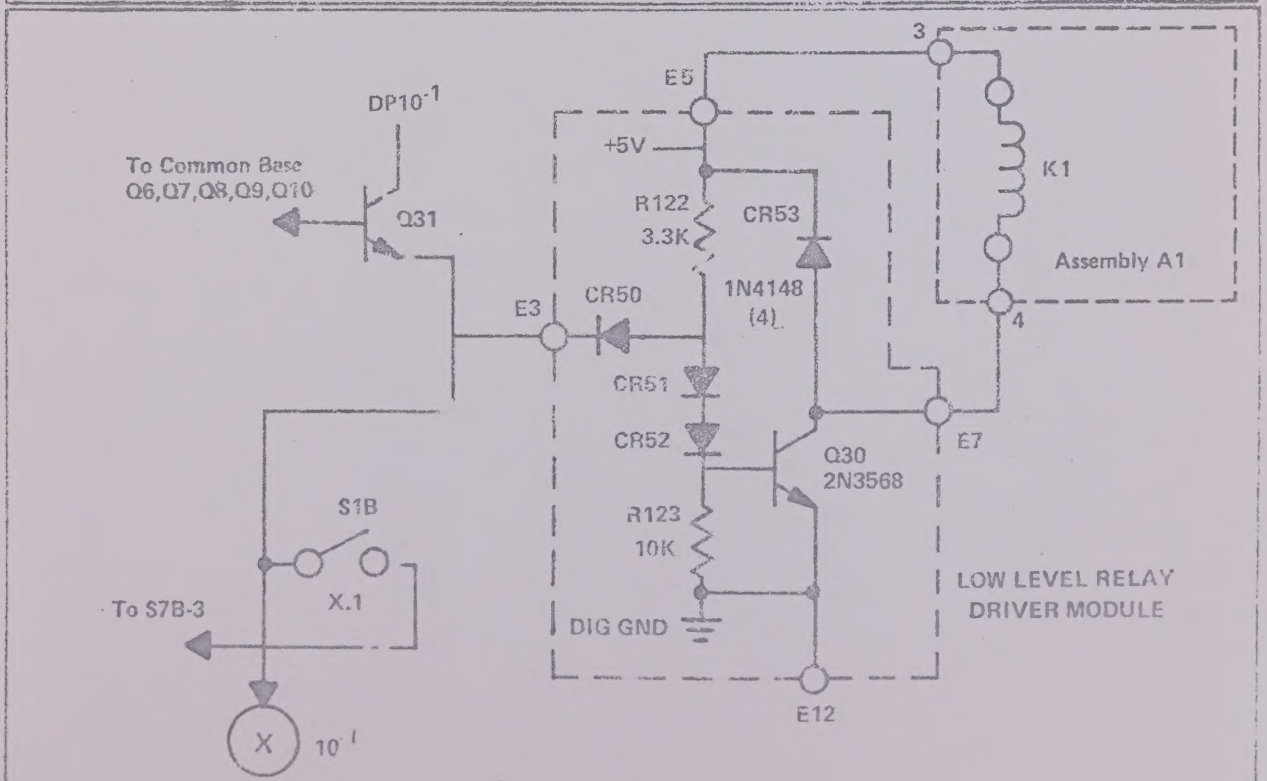

Fig. 6-4A Ranging Logic Modification for A1 Option

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